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BURGLAR ALARM SYSTEM

FINAL REPORT

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BURGLAR ALARM SYSTEM

FINAL REPORT

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TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF FIGURES

LIST OF FIGURES (Continued)

LIST OF TABLES

ABSTRACT

This document is a report of the hardware and software development effort for the Burglar Alarm System program funded by The Aerospace Corporation through a primary contract with the Law Enforcement Assistance Administration. The purpose of this effort was to develop all of the Burglar Alarm System components which were previously identified and specified as a result of the Systems Design Phase conducted earlier. A report on this earlier phase of the program is given as Report Number E-227 entitled "Burglar Alarm System Phase I Report," dated September 1975 by GTE Sylvania, Mountain View, California. The hardware subsequently developed and delivered conformed with all of the requirements and specifications as stipulated in the referenced report.

CHAPTER I. INTRODUCTION

This document is a report of the hardware and software development effort for the Burglar Alarm System program funded by the Aerospace Corporation under Contract Number 44368-V. The Aerospace Corporation in turn is under prime contract to the Law Enforcement Assistance Administration. This report fully defines all of the development effort which was subsequently undertaken after the Phase I Systems Design of the Burglar Alarm System program. Fully described in this report is the hardware and software development.

Chapter II is an Executive Summary of the results of the development effort. It is followed by Chapter III which fully describes the overall BAS system, its installation, operation, and the hardware details of each of the individual subsystems. Chapter IV describes in detail the software required to support the BAS system design. Software is resident in three of the BAS subsystems, namely the central processor, the entrance control, and the central station. Chapter V provides conclusions and recommendations as a result of the completion of the BAS program. Subsystems schematic diagrams and parts lists are given in Appendix A, while Appendix B provides flow charts for all of the system software and Appendix C provides a program listing for that same software.

CHAPTER II. EXECUTIVE SUMMARY

Specifications and requirements for the Burglar Alarm System were fully developed and documented during the system design phase of the BAS effort, and are recorded in Report Number E-277, entitled "Burglar Alarm System Phase I Report," dated September 1975 by GTE Sylvania, Mountain View, California. The hardware developed during this phase of the BAS program fully conforms to those requirements and specifications.

The BAS is composed primarily of six subsystems, i.e., the central processor, the entrance control, the sensor-transmitter, the external interface, the central station, and the local alarm. As its name implies, the primary purpose of the central processor is to provide the overall logic for the operation of the BAS. The processor represents the prime interface with the user. It allows the user to set in various operating modes, to change his four-digit combination which is used to access the BAS, and also provides a two-digit LED display of any trouble that has occurred in the system. It receives digital data which is transmitted over the power lines and subsequently, operates on it appropriately. The central processor also provides an interface to a remote monitoring facility via the external interface module.

The purpose of the entrance control subsystem is to preclude false alarms commonly generated by the user himself, i.e., walking into an armed system. The user may only gain entrance to his residence by punching in a predetermined four-digit code on a keyboard located on the outside of the residence. This data is then transmitted back to the central processor where it is decoded and compared with the preselected four-digit combination. If the proper combination was used, the central processor will disarm the system and send a signal back over the power lines to the entrance control to release the electric door strike at the front door. Furthermore, this provides the user with a simple keyless way to gain entry to the residence. In addition, the combination can be easily changed at the central processor. The entrance control also provides various other functions, i.e., arming of the system, sensing the door position at the entrance control, and also provides panic switches to allow the user to activate the alarm at the front door. There is also a tamper switch located at the keyboard which will sound an alarm if anyone attempts to remove the keyboard.

The sensor-transmitter's purpose is to provide the user with ease of installation. The user simply installs the sensor and runs a two-conductor wire to the nearest wall outlet where a sensor-transmitter is plugged in. The sensor-transmitter then transmits secure or alarm messages as the sensor switch is opened and closed. These signals are transmitted over the power lines to the central processor where appropriate action is taken. The sensor transmitters also transmit periodic status messages to allow the central processor to keep track of their proper operation. Each sensor-transmitter is uniquely identified in three ways: encoded on its digital transmission is the identity of the user himself, the type of sensor that it is, i.e., external, internal, fire, special, etc., and the identity of the specific sensor of a given type. The coding provides up to 16 unique identities for each type of sensor. The coding is easily established by the user simply through the insertion of code plugs inside the sensor-transmitters. Each sensor-transmitter accepts three code plugs to establish the above identifications.

As its name implies, the external interface interfaces the central processor to a remote monitoring site, such as a central alarm station. The external interface itself is simply a 600 baud full duplex modem which allows signals to be transmitted over telephone lines. Additionally, signals initiated from the central monitoring point are passed through the external interface and into the central processor.

Located at the other end of the telephone line is the central station monitor. The monitor developed for the BAS will accept signals from two separate BAS systems, since this is the total amount developed under this contract. The primary purpose of this central station monitor is to demonstrate feasibility of communicating with the central processors. When an alarm occurs and the processor is set in an external alarm mode, a digital signal is automatically transmitted back to the central station where it is decoded and the appropriate alarm light is displayed. Five types of alarms can be generated from each of the BAS's. They are fire, panic, intrusion, tamper, and special. In addition, the central station can interrogate each of the two systems to determine their status. An interrogation message is initiated to the selected BAS whereupon the appropriate BAS will respond with the appropriate status information.

The local alarm subsystem simply consists of a 10-inch bell located within a steel housing which is protected by two tamper switches. One tamper switch detects the opening of the bell box enclosure while the other tamper switch detects if any attempt is being made to dismount the entire system from its mounting surface.

It was not the intent of this development effort to finalize a product, but rather to demonstrate feasibility of the BAS concept. It was determined relatively early in the program that microprocessors would be used to implement the required system logic. At that time microprocessors started to appear on the market which were complete one-chip microprocessors with on-board clock, ROM, RAM, CPU, etc. These microprocessors can be sold at the present for less than $10 in reasonable quantities. It is projected that these same microprocessors or second generation single chip microprocessors will be available in the relatively near future in the two to three dollar range. This allows the system logic to be very sophisticated and yet can be implemented at a very low price. The microprocessor selected for developing the feasibility BAS systems was the INTEL 8080. The reason for its selection was basically two-fold: (1) it allows the use of external reprogrammable PROMs which allows flexibility during the development cycle since software can be easily changed and (2) the INTEL 8080 enjoys much software and hardware support. The negative side of using the INTEL 8080 is the fact that it needs a three voltage, well regulated power supply, as well as many support chips. This means that the feasibility models in no way reflect reduced sizes which will be achieved when a single chip microprocessor is employed in the design. Additionally, the power line transmitters and receivers were implemented in the feasibility models in terms of discrete circuitry. Additional cost and space savings will be achieved when the power line communications undergoes large scale integration. The entire BAS would, then, be very small and inexpensive yet would still provide many sophisticated functions to the user.

CHAPTER III. BAS HARDWARE DEVELOPMENT

3.1 BAS DESCRIPTION, INSTALLATION AND OPERATION

The purpose of this section is to provide an overall description of the developed BAS configuration. This section will define the interface between the various subsystems and between the system and the user. Design details of each of the subsystems are given in subsequent sections. An artist's concept of the overall system is shown in Figure 3-1. Shown in the lower right hand portion of the illustration is the processor which is central to the entire system. As its name implies, it processes information received from all of the sensor transmitter units and the entrance control unit and controls the modes of operation of the system. The panel layout, illustrated in Figure 3-1, is only functional and is in reality configured as a result of the human engineering effort with GVO Incorporated.

In order to eliminate a major portion of the system wiring and its associated expense, sensors installed throughout the house may simply be wired to the nearest wall outlet where a sensor-transmitter is inserted into the outlet. The sensor-transmitter, upon receiving an alarm condition from the sensor, will format a specific alarm message and relay this message via the power lines to the processor. The processor will then initiate the appropriate action depending upon the setting of the operating mode switches.

The purpose of the entrance control is to preclude false alarms caused by carelessness on the part of the user. The majority of false alarms are caused simply by the user's failing to disarm the system prior to entry. The entrance control consists of a keyboard installed on the outside door jamb. In order to enter the premises, the user must punch in his previously selected four-digit code which is transmitted via the power lines to the processor. If the code is valid, the processor will disarm the system and send a strike release signal back to the door to allow the user to enter.

There are three basic alarm mechanisms which the processor may initiate. The first of these is the sounding of a local alert signal which is incorporated into the processor and there can also be an optional local alert module. This module is illustrated in the upper right hand corner of Figure 3-1. It is used to alert the user of an intrusion or a fire condition while he is located within the house.

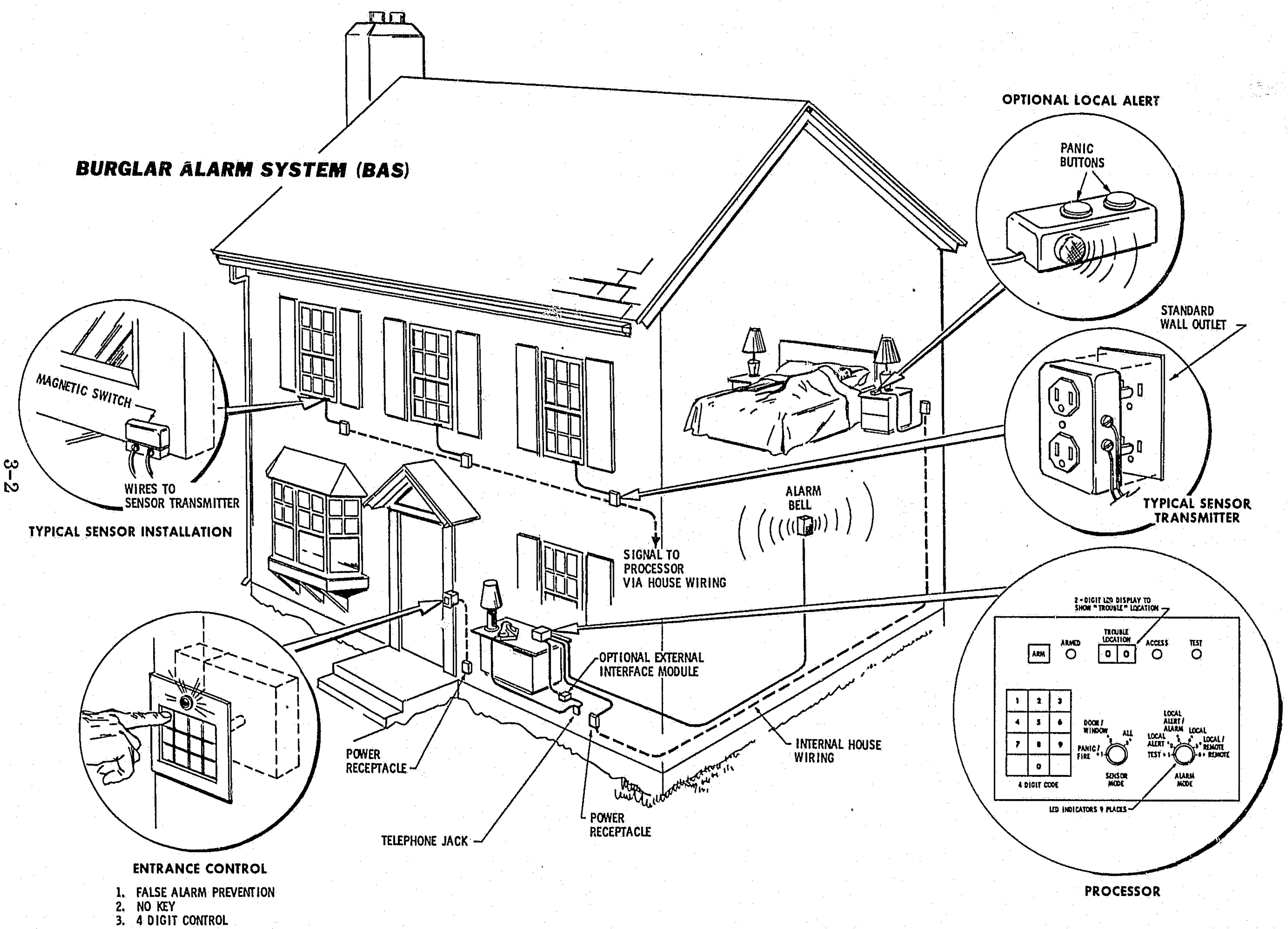


Figure 3-1. Overall Concept

3.1 (Continued)

The second alarm mode available is that of initiating the loud local alarm, i.e., the bell. This sounding device is hardwired from the processor to the sounding device's external location.

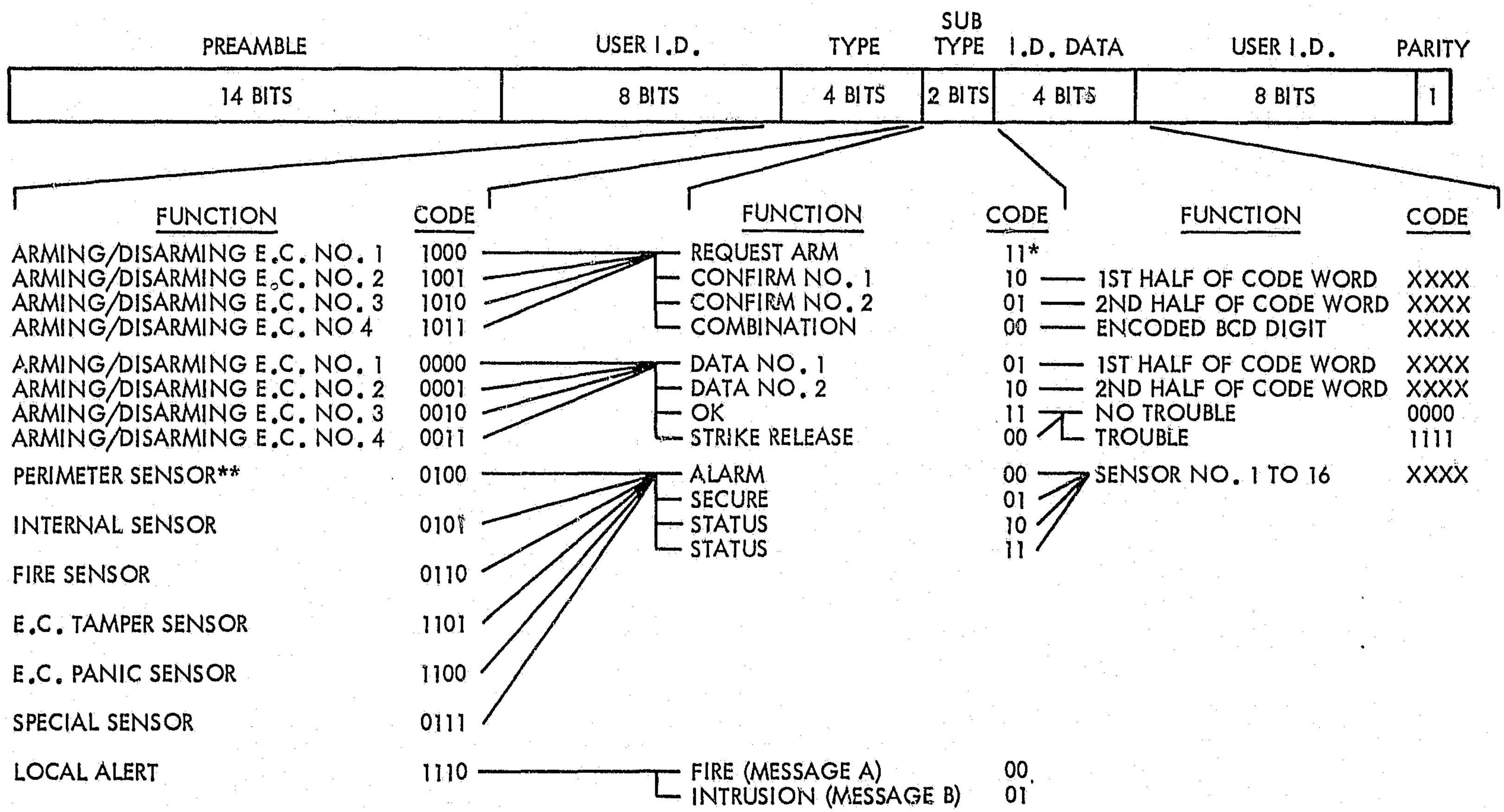
The third alarm alternative is that of initiating a signal which can be monitored at a central monitoring facility. This requires an optional external interface module which interfaces the processor to the telephone lines.

The following paragraphs describe the system operation in detail. It should be noted that the description is centered around a fully configured BAS system, i.e., all of the capabilities of the system will be described. It should be further noted that manufacturers of BAS are not forced to configure the system with all of the available functions. The reason he may not do this is to save costs on peripheral equipment required, such as switches, indicator lights, etc. These functions, however, will be available on production developed chip whether a manufacturer chooses to fully utilize its capabilities or not.

3.1.1 Message Formatting

The BAS system utilizes a digital FSK signal for intrasystems communications. Figure 3-2 shows the primary BAS message structure. The first fourteen bits are used as a preamble to establish bit synchronization. Eight bits are used at the beginning and end of the message bits to uniquely identify a particular user.

Sixteen bits were statistically selected for this identification based upon the number of users which may share the same secondary of a power distribution system. The first four bits following the first eight bits of the user identification code are used as the "type" field. The type field identifies which one of four possible entrance controls a signal is coming from or going to and also establishes whether a sensor transmitter is performing a perimeter, internal, fire, tamper, panic, or special sensor function. Following the four-bit type field is a two-bit "subtype" field. The subtype field indicates the nature of the message being transmitted to and from entrance controls and sensor transmitters. The nature of these messages will be explained later in this subsection. The two-bit subtype field is then followed by a four-bit ID/data



* I.D./DATA FIELD NOT USED

** PERIMETER SENSORS NO. 12, 13, 14, & 15 ARE E.C. DOORS NO. 1, 2, 3, & 4 RESPECTIVELY

Figure 3-2. BAS Message Format

3.1.1 (Continued)

field which is used by a sensor-transmitter to uniquely identify that particular transmitter and is used by the entrance control and processor for the transmission of a four-bit data word. This ID/data field is then followed by the remaining eight bits of the user identification code which in turn is followed by a parity bit for a total of 41 bits.

3.1.2 Installation

The majority of the BAS installation is extremely simple and can be done by the user himself. Sensor-transmitters are simply located at the wall outlet which is closest to the point at which the sensor is installed. The processor is plugged into a convenient location, such as a position near to where the bell will be mounted and/or near a telephone jack. The most difficult part of the installation consists of installing the entrance control and the alarm bell. In order to install the entrance control, it is only necessary that a single one-half inch diameter hole be drilled through the door jamb over which a keyboard will be surface mounted. The cable from the keyboard is inserted through the hole and interconnected to an electronic package which is surface mounted at the other end of the hole through the door jamb. The electronics housing contains an electric strike, a recessed arming switch at its edge, two panic buttons and a magnetic reed switch for sensing the door's position. A mating module, which contains a spring loaded bolt, is also surface mounted at the back side of the door. A multi-conductor cable is then run from the electronics housing to a unit which plugs into the nearest wall outlet.

Installing the bell simply consists of running a four-conductor cable from the processor to the bell's location. The bell box is surface mounted on an external wall of the house. Manufacturers configuring the system for apartment use may elect to incorporate the local alarm sounding device into the processor box to further ease installation and cost. If an optional external interface is desired, it only requires a cable to be run from the processor to the external interface module and from the interface module to a telephone jack. The vast majority of users can easily install the system themselves or they may elect to get the services of a professional installer. Because of the ease in which the system is installed, a professional installer could easily install the system within one, or at the most, two hours depending upon the number of sensors used in the system.

3.1.2 (Continued)

The following paragraphs will deal with the system in its operational use. These will be discussed in a chronological sequence and features of the system will be pointed out as the user goes through the operating sequence.

3.1.3 Initialization and Code Plug Insertion

When the user gets ready to put his system into operation, he opens the processor and sees what is illustrated in Figure 3-3, which is a photograph of the feasibility model. There is a series of dual in-line package code plugs as shown in the photograph, and a start/run switch. The rows of code plugs marked "external," "internal," "fire," "special" and "entrance" are all inserted into their sockets when the system is delivered. The user ID code plugs are supplied in a separate plastic bag and one of these is inserted into the two receptacles entitled "user ID." In order to establish the coding of a particular transmitter, it is necessary to plug three plugs into the sensor-transmitter itself.

Two of these plugs are user ID code plugs and the other plug is one which is extracted from the processor. If for instance the sensor-transmitter would be used to monitor a magnetic switch on the back door, then the code plug number one under the "external" column would be extracted from the processor and plugged into the sensor-transmitter at that location. Through the absence of that code plug, the processor then knows that it must keep status of an external sensor number one. These code plugs establish the sensor transmitter's unique identity and its function. When the user installs the code plug in each transmitter, he makes a note as to the numerical identification of each of the transmitters, i.e., whether it is one, two, three, four, etc. This will allow him at a later date to properly interpret the trouble identification code which is displayed on a two-digit code display located on the processor front panel. The trouble indicator will indicate the number of the particular sensor-transmitter which is causing trouble or will give a code indicating other trouble in the system. A list of these trouble codes is given in Table 3-1.

After each of the system sensor-transmitters and entrance control modules has received its code plugs, the system is ready to be brought into operation. This is done simply by placing the start/run switch into the start position and plugging the processor into the nearest ac outlet. This initializes the logic of the system and sets RAM memory to zero. In order to make the system fully operational, then, it

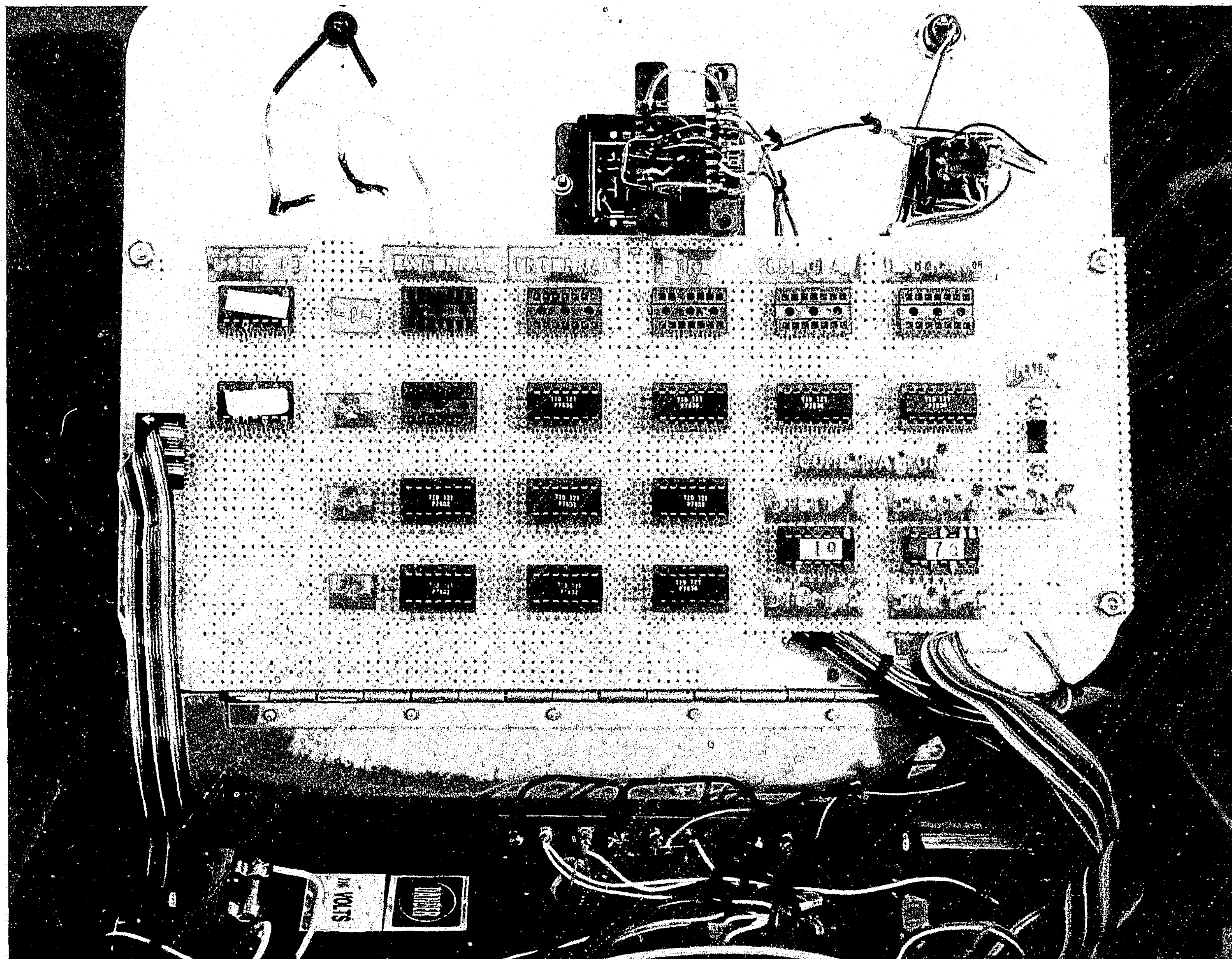


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Figure 3-3. BAS Processor – Internal View

Table 3-1. Trouble Indication and User/System Error Codes

Sensor Trouble or Alarm Codes

Code	Sensor-Transmitter Identification
01	- * EXTERNAL SENSOR # 1
02	- * EXTERNAL SENSOR # 2
03	- * EXTERNAL SENSOR # 3
04	- * EXTERNAL SENSOR # 4
13	- * ENTRANCE CONTROL # 1 DOOR
14	- * ENTRANCE CONTROL # 2 DOOR
17	- * INTERNAL SENSOR # 1
18	- * INTERNAL SENSOR # 2
19	- * INTERNAL SENSOR # 3
20	- * INTERNAL SENSOR # 4
33	- * FIRE SENSOR # 1
34	- * FIRE SENSOR # 2
35	- * FIRE SENSOR # 3
36	- * FIRE SENSOR # 4
49	- * SPECIAL SENSOR # 1
50	- * SPECIAL SENSOR # 2
65	- * ENTRANCE CONTROL # 1 PANIC
66	- * ENTRANCE CONTROL # 2 PANIC
69	- * ENTRANCE CONTROL # 1 TAMPER
70	- * ENTRANCE CONTROL # 2 TAMPER
73	- * PROCESSOR OR BELL TAMPER-
74	- * JAMMING DETECTOR FOR EITHER POWER LINE OR MODEM (INTERNAL SENSOR ALREADY IN PROCESSOR)

* NOTE: - FLASHING DIGIT DISPLAY INDICATES AN ALARM
- STEADY DIGIT DISPLAY INDICATES A NON-REPORTING SENSOR OR A SENSOR LEFT IN THE ALARM STATE

User/System Error Codes

Code	Condition
80	- CAUTION - FAILURE IN ENTRANCE CONTROL # 1 COMMUNICATION
81	- CAUTION - FAILURE IN ENTRANCE CONTROL # 2 COMMUNICATION
84	- ARMING ABORTED - SYSTEM WILL NOT ARM FROM PROCESSOR (ONLY AT AN ENTRANCE CONTROL) IN LOCAL ALARM, LOCAL/REMOTE, OR REMOTE MODES
85	- CAUTION - SYSTEM ARMED FROM PROCESSOR IN TEST OR LOCAL ALERT MODES
86	- CAUTION - POWER LINE OR MODEM RECEIVER PARITY ERROR OR SENSORS REPORTING WHICH ARE NOT RECOGNIZED BY THE SYSTEM (CODE PLUGS ARE STILL IN PROCESSOR)
87	- CAUTION - POWER HAS BEEN RESTORED
88	- CAUTION - SYSTEM ARMED FROM AN ENTRANCE CONTROL IN LOCAL ALERT MODE
89	- ARMING ABORTED - SYSTEM WILL NOT ARM FROM AN ENTRANCE CONTROL IN FIRE/PANIC, TEST, OR ACCESS MODES

3.1.3 (Continued)

is only necessary to place the start/run switch in the run position. Next, the user simply plugs in his two "combination" code plugs which establishs the four-digit combination to be used at the keyboards. The processor box is then closed and the system is operational.

3.1.4 Access Mode and Mode Selector

After the system has been put into operation through the above steps, the user may select any mode of operation he desires. Any changes of the processor setting must be preceded by the user punching in his four-digit code at the processor front panel. When he does this, the processor goes into what is termed an "access" state. The first thing that this state does is disarm the system, if it is armed. The length of period for the access state is dependent upon two things, one is a sixty-second timer and the other is whether the tamper switch on the processor cover is in a secure position. The access period allows the user to open the cover of the processor without causing a tamper alarm. The last of those two events, the 60-second timer or the closing of the front panel, will cause the system to go out of the access mode; an indicator light on the front panel indicates to the user whether or not he is in the access mode. This light is illustrated in Figure 3-4 which is a photograph of the processor front panel. By pushing in his four-digit code, the user may then reset his code by opening the front panel and changing the combination code plugs or he may temporarily disable all of the tamper switches in the BAS system. The user may also shut the entire system down by disconnecting ac power. The mode selection switches will only be read by the processor logic at the termination of the access period. Any subsequent change in the position of the mode selection switch will not change the operating mode of the processor. In order to change that mode, it is necessary for the user to punch in his four-digit code prior to setting the switches.

LED indicators display the mode of operation of the processor in the event that the switch positions have been changed. These indicating LED's can be illuminated by pushing the "Illuminate Trouble Indicator" button without punching in the four-

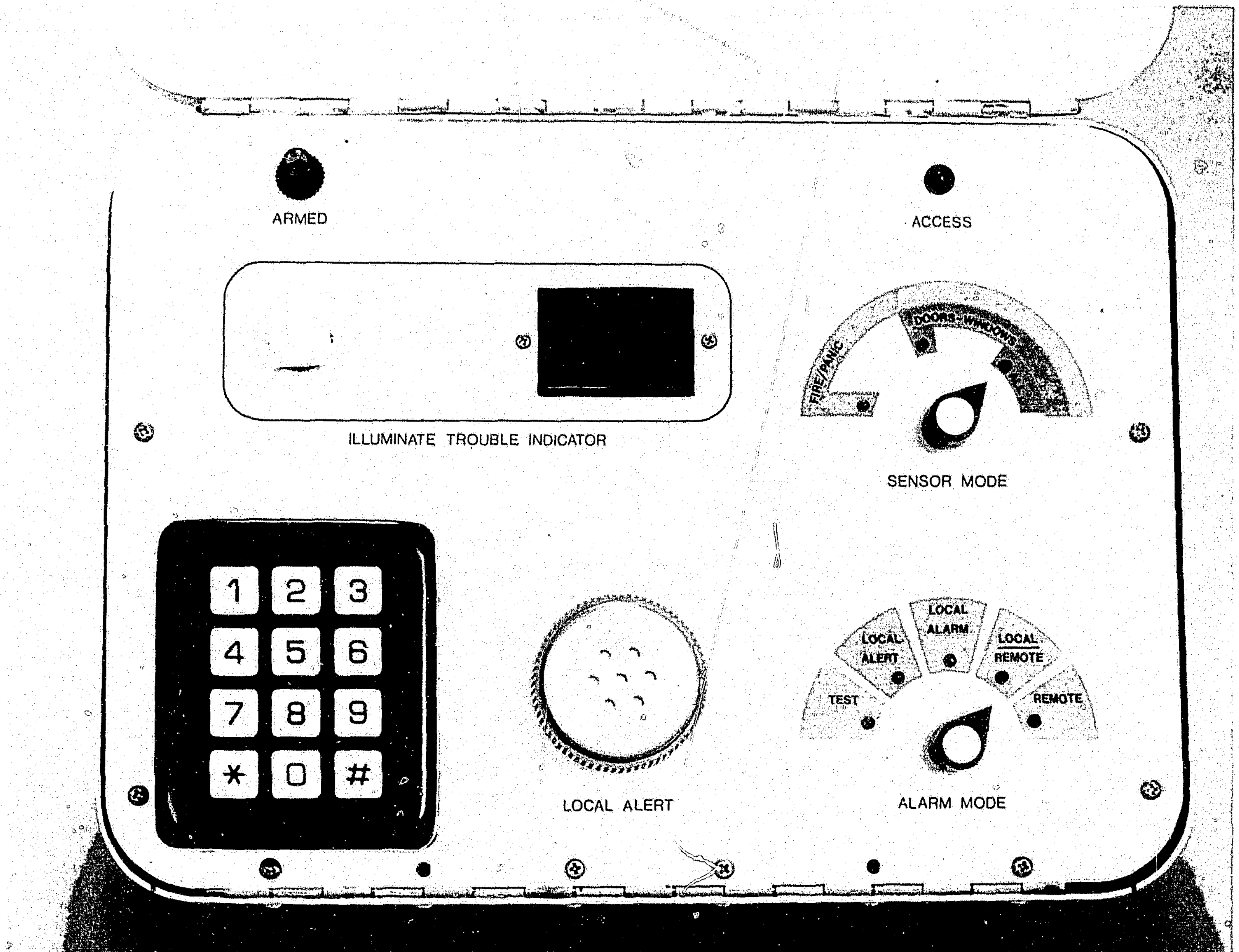

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Figure 3-4. BAS Processor – Front Panel

3.1.4 (Continued)

digit code. Also indicated at this time is the numerical indication of any trouble that exists in the system. If the four-digit code is punched in and then the "Illuminate Trouble Indicator" button is depressed, the system will be armed and an indication of that arm state will be given through another LED indicator above the button.

The two mode switches allow the user a high degree of flexibility in the way he uses the system. A three position sensor mode switch allows him to select three different modes for monitoring sensors. The panic and fire sensors are being monitored in all three modes of operation even when the system is not armed. By placing the sensor mode switch in position number two, the door and window sensors, i.e., perimeter sensors, are added to the panic and fire sensors. These sensors, however, are only monitored when the system is armed. By placing the sensor mode switch in position number three, all of the sensors in a residence are monitored including the internal sensors such as switch mats, volumetric devices, etc. Again, these burglary sensors are only monitored when the system is armed.

The alarm mode switch allows the user five different alarm reporting schemes. In position number one, alarm indications are only given via the local alert and a test light on the front panel; this allows the user to test all of the various sensors in the system. In position number two, only the local alert is sounded; in position three, only the local alarm, that is the loud sounding device, is actuated; in position four, both the sounding device and the signal sent to a remote monitoring station is initiated. This remote function, of course, can only be used if the user has elected the optional external interface module. In position five, only a silent alarm signal is sent to the central monitoring station.

3.1.5 System Arming

The BAS system can be armed at two locations - at the front panel of the processor or the entrance control. If an entrance control is incorporated into the system and the system is armed at the front panel, the logic in the processor precludes arming of the system in any of the external alarm modes, i.e., alarm mode switch positions three, four and five. This is done in order to preclude false alarms. A system with an entrance control would normally only be armed from the processor front panel for protection of the individual while he is within the residence. If, for instance, he

3.1.5 (Continued)

wanted to monitor all of his sensors during the evening hours, he would place the sensor mode switch into position three (all) and his alarm mode switch in position two (local alert). He would then punch in his combination and activate the arm switch. Each time one of the sensors is activated, the local alert will sound. The user then has the option of investigating the source of the alarm and/or to activate a panic button, which will cause a local alarm to be actuated. Not allowing the user to arm the system in any external alarm mode from the processor front panel will negate the possibility of members of the household inadvertently setting off false alarms as they move about within the residence.

When an entrance control is incorporated into the BAS system, the user may arm the system at the front door. He accomplishes this by opening the door and exposing the recessed button located on the edge of the electronic package of the entrance control which is surface mounted on the door jamb. He simply presses the button and closes the door behind him. He then glances at the LED display on the keyboard to get a 20 second indication of whether the system has successfully armed. A successful arming sequence is indicated by a steady glow of the LED indicator for a 20 second period. If there is trouble within the system, the LED indicator will blink, alerting the user to this fact. Trouble will be indicated if, for instance, any of the intrusion sensors have been activated, such as an open protected door. The user, upon seeing the blinking LED indicator, may still elect to leave and if he does so, the processor will arm all of the non-activated sensors. The processor will not monitor any of the sensors indicating trouble. If the user, on the other hand, wishes to correct the trouble, he simply punches in his four-digit access code at the front door which will allow him to reenter and go to the processor to determine the source of the trouble. In order to do this, all he has to do is to push the "Illuminate Trouble Indicator" button and the numerical representation of the offending sensor or condition will be displayed on the two-digit LED display. If there are multiple troubles, they will be sequentially displayed each time the button is pushed. The user may then take corrective action, such as closing the rear door. A trouble indication will also be given if the user has armed his system from the front door with the sensor mode switch in position one (panic/fire) or with the alarm mode switch in position

3.1.5 (Continued)

one or two (test and local alert). After the user corrects the trouble, he will then go through the same exit sequence and will then get a continuous five second illumination of the LED at the keyboard to indicate all of the trouble has been cleared and the system is fully armed.

At this point, some processor logic which is completely "invisible" to the user will be described. Additional logic is included in the processor and the entrance control to deal with a vulnerability in the system. This vulnerability, about to be described, is a result of a widely proliferated system which the BAS potentially will be. The vulnerability results in the fact that the four-digit combination is transmitted over the power lines to the processor which, if valid, will cause the processor to disarm and send a strike release signal back to the entrance control. A potential intruder, through the use of another BAS system and a tape recorder, could simply observe the time in which the intruder entered his premises and record the signals that were transmitted over the power lines. All the intruder would have to do to gain access to the user's residence is play the recording back onto the power line when the user was away. This signal, when received by the user's processor, would not only disarm his system but would also open the front door for the intruder. Such a technique would be a universal key to anyone using a BAS system. In order to avoid this vulnerability, we use the capability of a microprocessor to further encode the user's combination data. This is done as follows: when the user arms his system at the front door, a dialogue between the processor and the entrance control is established. After the arming button at the entrance control has been depressed and the door is closed, a "request for arm" message is sent from the entrance control to the processor. This message, along with the others to be discussed, are shown in the BAS message format in Figure 3-2. The processor, upon receipt of the request for arm signal, generates an eight-bit pseudorandom code. This means that there are 256 possible eight-bit combinations that can be generated. The processor will then transmit the first four bits of the eight-bit code to the entrance control in the ID/data field of the message. The subtype bits will indicate that these four bits are "data number one." The entrance control will then transmit a "confirm number one" message back to the processor echoing the same four bits in the ID/data field. If the processor receives an incorrect data number one word, then it will reissue the data number one code until it is received at the entrance control and properly transmitted back to the processor. The processor will then repeat the same sequence with the last four bits of the eight-bit code word making sure that the entrance control has received it properly. When both four-bit code words have been properly transferred from the processor to the entrance control, the processor will eliminate the old code bits and load the new code bits into a storage register, and will transmit an "OK" signal to the entrance control to do the same. The two four-bit groups are now located at both the processor and the entrance control. This entire sequence takes approximately 3 seconds. These code words are now used to further encode the combination data being sent on the power lines. This is done by exclusive ORing the combination digits with the code data. Figure 3-5 indicates the characteristics of the exclusive OR'd function. When this data, which is the combination digit, is exclusive OR'd with the key word, which is the four-bit code word, an encoded signal is generated. This signal is then transmitted from the entrance control to the processor. The processor then takes the encoded message and exclusively OR's it with the code word to retrieve the original data or combination digit. The combination digits are alternately exclusively OR'd with the two four-bit code words. In order that the user does not have to enter his combination in a synchronous fashion, i.e., he must press all four digits and not restart the combination after, for instance, the third digit, either pattern of alterations are accepted as a valid code by the processor. In other words, the processor will decode a one-two, one-two, one-two pattern or a two-one, two-one, two-one pattern and only require that the last four digits decoded compare properly with the combination set into the processor. By accepting either pattern, the number of possibilities are reduced from 256 to 128 which is felt to still be quite safe. Now the intruder would have to actually attempt to decode data on the power line in order to gain entry. This level of sophistication is beyond the capabilities of the intruder since there are two unknowns in the system, i.e., the combination and the code words. He would have to successively observe a total of 128 accesses before he could predict a pattern. As was stated earlier, this entire process is invisible to the user, but serves to eliminate a potentially very vulnerable situation.

In the instance where no entrance control is used in the system, the processor, through sensing the presence of all of its entrance control plugs, resorts to another mode of operation. When no entrance control is incorporated, the processor will

DATA	$\oplus$ KEYWORD	= ENCODED
0	0	0
1	0	1
0	1	1
1	1	0

ENCODED	$\oplus$ KEYWORD	= DATA
0	0	0
1	0	1
1	1	0
0	1	1

Figure 3-5. Modulo 2 Addition

3.1.5 (Continued)

allow a period of approximately 45 seconds for the user to exit without causing an alarm. Upon reentry, the processor will allow approximately the same period of time to disarm the system by punching in his four-digit code at the processor front panel. As soon as the door is entered, a local alert at the processor and in any optional local alerts will sound to alert the user that the alarm will be initiated unless he disarms the system. From a system standpoint, this is not a desirable arming or disarming technique, but is the only one available when an entrance control is not used.

3.1.6 Armed and Non-Armed System Operation

After the system has been armed, as described in the previous section, sensors will be monitored as a function of the sensor mode switch setting and the pruning operation which may or may not have taken place at the time the system was armed. When a sensor-transmitter is activated, it sends out five alarm messages spaced at one minute periods. This assures with a very high degree of probability that the alarm message will be received by the processor. The "alarm" message is only one of three different types of messages that are transmitted by the sensor-transmitters. The other two messages are "secure" messages and "status" messages. The "secure" message is transmitted at the time that the sensor is deactivated, such as when a door is closed. These messages also are transmitted five times at one minute periods. This allows the processor the capability to keep track of the status of all sensors in the system. Furthermore, it provides protection against the intruder who attempts to jam the communication system. This is accomplished by simply monitoring the phase lock circuit on the BAS receiver and coupling that information with the "secure" messages transmitted by the sensor-transmitters. The anti-jamming function will be set only to produce an alarm if jamming energy is present for a period of at least three minutes. An intruder then might attempt to jam the power lines and gain entrance during this period of time. He must, however, remove his jammer from the line before the three minute period is up or an alarm condition will be created. If he does this and the door is not closed, then alarm messages are still being transmitted and will be received by the processor and an alarm will be initiated. If the intruder closes the door and removes the jammer, then "secure" messages will be transmitted to the processor and the processor will initiate an alarm based upon the existence

3.1.6 (Continued)

of a "secure" message since it had not previously received an "alarm" message, i.e., the door could not have been closed unless it had been opened. Without this feature, it would be very easy to manufacture jammers which would basically be a key to defeating any BAS system. Furthermore, it should be noted this feature can be provided with no additional system cost since the phase lock circuit already exists as does the five-minute timer in the sensor-transmitters. The little addition in logic required in the processor can easily be handled by the existing capabilities of the microprocessor.

The third type of message transmitted from the sensor-transmitters are "status" messages. These messages, as its name implies, allow the processor to keep track of the fact that sensors are alive and well. The "status" messages are sent at a rate of one every hour and the processor will require that two consecutive "status" messages be missed prior to declaring a trouble indication. This will allow the user to be able to determine within a period of two hours whether a sensor transmitter has failed or has been disconnected from the system. To further protect against the unauthorized removal of a sensor-transmitter from its wall outlet, the position of the center mounting screw will be monitored. If the screw is withdrawn, a microswitch activated by a cam on the captive screw will cause a series of "alarm" messages to be transmitted. This also allows the user to check out his system by withdrawing the mounting screw. The mounting screw then becomes a combination of a test switch and a tamper switch. This provides a way for the user to check out the integrity of the system when certain types of sensors are used which cannot easily be activated, such as heat sensors.

Tamper switches are located at the entrance control keyboard, the processor cover and the cover for the local alarm module. The activation of any of these tamper switches will cause an alarm initiation whether the system is armed or not. The user may deactivate the tamper circuit by punching his authorized code at the processor and opening the processor door. This act will deactivate all tamper switches until the processor door is closed.

3.1.7 Secure Disarming

In a BAS system, which incorporates the entrance control, it is extremely simple to disarm the system. All the user must do is press in his four-digit code at the front door which will be encrypted by the entrance control, transmitted back to the processor,

3.1.7 (Continued)

and if proper, the processor will disarm the system and send a strike release signal back to the front door to open it. If while the user was absent an alarm condition occurred or trouble occurred within the system, the user would be notified by a flashing light at the entrance control keyboard that something was wrong. The user may then go to the processor and push the "Illuminate Trouble Indicator" button in order to be able to read out the two-digit LED display. If an alarm condition has occurred, the display will flash intermittently with the number of the alarmed sensor-transmitter being displayed. If trouble occurred within the system, then the two-digit LED display will come on continuously, displaying the number of the troubled sensor or the code for other trouble such as a jamming attack.

If the BAS system does not have an entrance control associated with it, the system must be disarmed at the processor. As soon as the user enters the premises, he will hear a local alert. This local alert prompts the user to go to the processor to punch in his four-digit code in order to disarm the system. Failure to do this in a time period of 25 seconds will result in an alarm condition.

The following subsections describe the electrical and mechanical design of each BAS subsystem.

3.2 CENTRAL PROCESSOR

3.2.1 Functional Description

The central processor is the brains of the basic burglary alarm system. Its purpose is to simply input information, make decisions in software based on this data, and then to output information in the forms of lights, alarms, or messages. A block diagram of the central processor is shown in Figure 3-6 and a photograph of the processor with the local alarm and internal interface are shown in Figure 3-7.

All data is input through one unidirectional input port, and a bidirectional communication interface. The data that is brought in through the input port is open or closed switch information and is one of ten 8-bit words that tell the microcomputer which sensor code plugs are installed, which key at the keyboard is depressed, what sensor mode and alarm mode have been selected, tamper switch status, start/run switch position, illuminate arm switch position, the user ID, the system combination, and the clock and flags associated with the communication interface. Messages are input

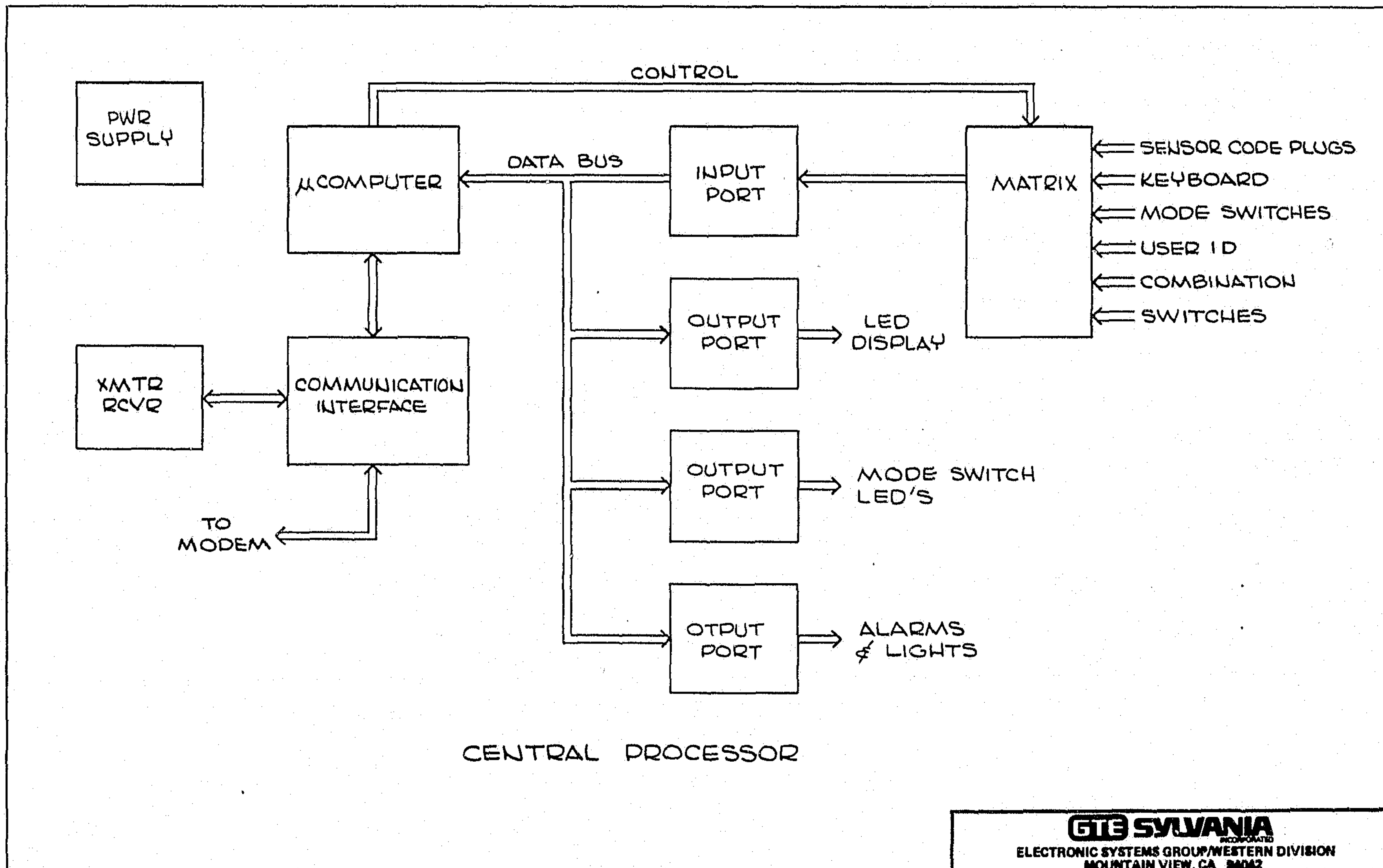

Figure 3-6. Central Processor Block Diagram

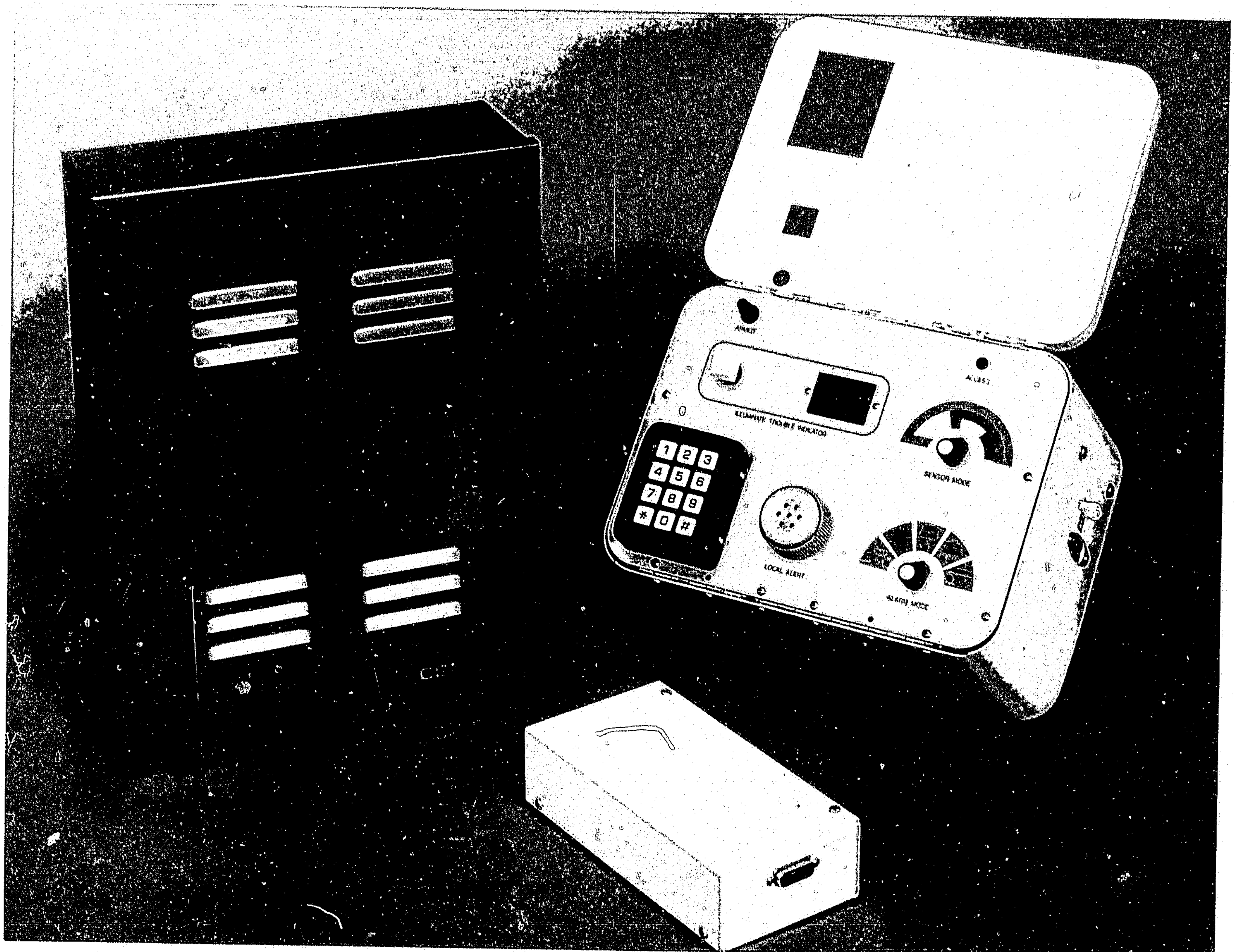

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Figure 3-7. Local Alarm, External Interface and Central Processor

3.2.1 (Continued)

to the microcomputer through the communication interface in a bit by bit fashion. These messages may come from the power line or the modem. The modem is used for communication with the remote central station.

All data is output through three unidirectional output ports and the bidirectional communication interface. Output port number 1 is used to output BCD data to the digital LED display which indicates the location of trouble in the system. Output port number 2 is used to output the alarm and sensor modes to the switch LEDs. Output port number 3 is used to light the armed or access lights, turn on the local alert or local alarm, and raise flags to control the communication interface.

All of the I/O circuitry and the communication interface is located on a single wire-wrapped circuit card. The microcomputer is on a single printed circuit board. The receiver and transmitter are also located in the central processor and are on separate printed circuit cards. There is also an alarm bell driver circuit on a vector board located in the central processor. The power supply provides +12V, -12B, and +5V. The -5V is derived from -12V on the alarm bell driver circuit card.

3.2.2 Circuit Description

3.2.2.1 Microcomputer

The microcomputer is based on an INTEL 8080A Central Processing Unit, memory, and associated control chips. A schematic of this board is shown in SK00-3415 in Appendix A.

The 8080 address lines, A0 through A15, are used to select memory locations for reading or writing to memory and for selecting input and output ports. With A0 as the least significant bit, addresses 0 through 1023 are used to select words stored in U5, 1024 through 2047 are used to select words stored in U6, and 2048 through 3071 are used to select words stored in U9. U5, U6, and U9 are INTEL 8708 ultraviolet eraseable PROMs. Addresses 3072 through 3327 are used to read or write to locations in RAM, which is comprised of two parallel four-bit slices. Address lines A10 and A11 are decoded by U1 which is an INTEL 8205 one-of-eight decoder and is used to perform the actual selection of U5, U6, U9, or U7 and U8.

3.2.2.1 (Continued)

Address lines A0 through A9 are then used to select the location on U5, U6, or U9, and address lines A0 through A7 are used to select the location in RAM (U7 and U8). The address buss is also made available at JP1, and A12 through A15 at P1 for use in I/O operations.

The 8080A bidirectional data buss lines D0 through D7 are buffered by an INTEL 8228 which is also used to generate synchronized control signals that tell whether an operation is a memory read or write or a peripheral input or output. The data buss and control lines are also made available at R2 and P1 for use in I/O operations.

The 8224 chip, U3, is used to generate two two-phase clocks for the 8080A at a frequency which is one-ninth of the crystal frequency. This chip is also used to generate a synchronized reset signal when power is applied. Timing and waveforms can be obtained from the INTEL 8080A users manual.

The following subsections discuss the circuit operations of the Central Processor subsystems, i.e., the microcomputer, the I/O matrix, the communication interface, the code plug board, the front panel and the power supply.

3.2.2.2 I/O Matrix

The purpose of the I/O matrix is to input multiple eight-bit words into a single input port and to output multiple eight-bit words from the same eight-bit data buss. These eight-bit input words represent switch positions and the output words represent off/on information for various indicator lights, local alert, local alarm and binary code for display on the two digit trouble indicator. The following description makes reference to schematic SK00-3421 in Appendix A.

All information, with the exception of receiver and modem data, is input through U1, an INTEL 8212 latching tri-state port. This information consists of nine eight-bit data words and is selected one at a time by U10 and U11, which are INTEL 8205 one-of-eight decoders. These decoders have one-of-eight active low outputs and use address lines A12 through A15 for selection. All input data lines are pulled up to 5V (a logical one) by resistors R1 through R9 inclusive. The data lines are pulled low by applying a ground to them through the appropriate switch and an open circuit allows the resistors to pull the line to 5V. The INTEL 8212 is also used to output data through U2, U4, and U5.

3.2.2.2 (Continued)

The bidirectional shift register U3 is used to input and output information to and from the transmitter/receiver and modem in a bit-by-bit manner.

3.2.2.3 Receiver

The function of the receiver is to recover data and clock signals which have been transmitted from remote sensors, the central processor, or the entrance control. Building power distribution lines normally provide the signal path from transmitter to receiver. The receiver operates continuously, but the transmitters operate in low duty cycle bursts. This means that most of the time the only input to the receiver is noise from the power line. When a data burst from one of the transmitters appears on the line, the receiver must quickly adapt to a coherent signal so that essential data and clock signals are not lost. Another problem is that the RF input level may vary over a 70 dB range and there may be severe impulse noise interference. To obtain good performance under these conditions, a moderately elaborate receiver is required. The receiver block diagram is shown on Figure 3-8, and the schematic diagram is given in Appendix A as SK00-3411.

Frequency selectivity is obtained from the input line coupling network which functions as a bandpass filter. The amplitude versus frequency response of this network is shown on Figures 3-9 and 3-10. Shunt diodes are connected to the output end of the network to prevent damage to the following circuits by high level transients from the power line.

Receiver RF gain and amplitude limiting is obtained from U8, which is a high gain four-stage amplifier designed for FM receiver IF use. The output of the amplifier-limiter is coupled to the FM demodulator with a single pole bandpass filter tuned to 170 kHz. The function of this filter is to attenuate broadband noise generated in the amplifier-limiter.

A phase locked loop frequency discriminator is used for demodulation. All of the active circuits of the loop are contained in U9. U9 also contains an extra phase detector which is used with comparator U10 and flip flop U15B to make a phase lock indicator. The output of this indicator circuit is available as a message flag to indicate reception of a coherent signal. The output of the FM demodulator feeds the clock recovery and the bit detector circuits.

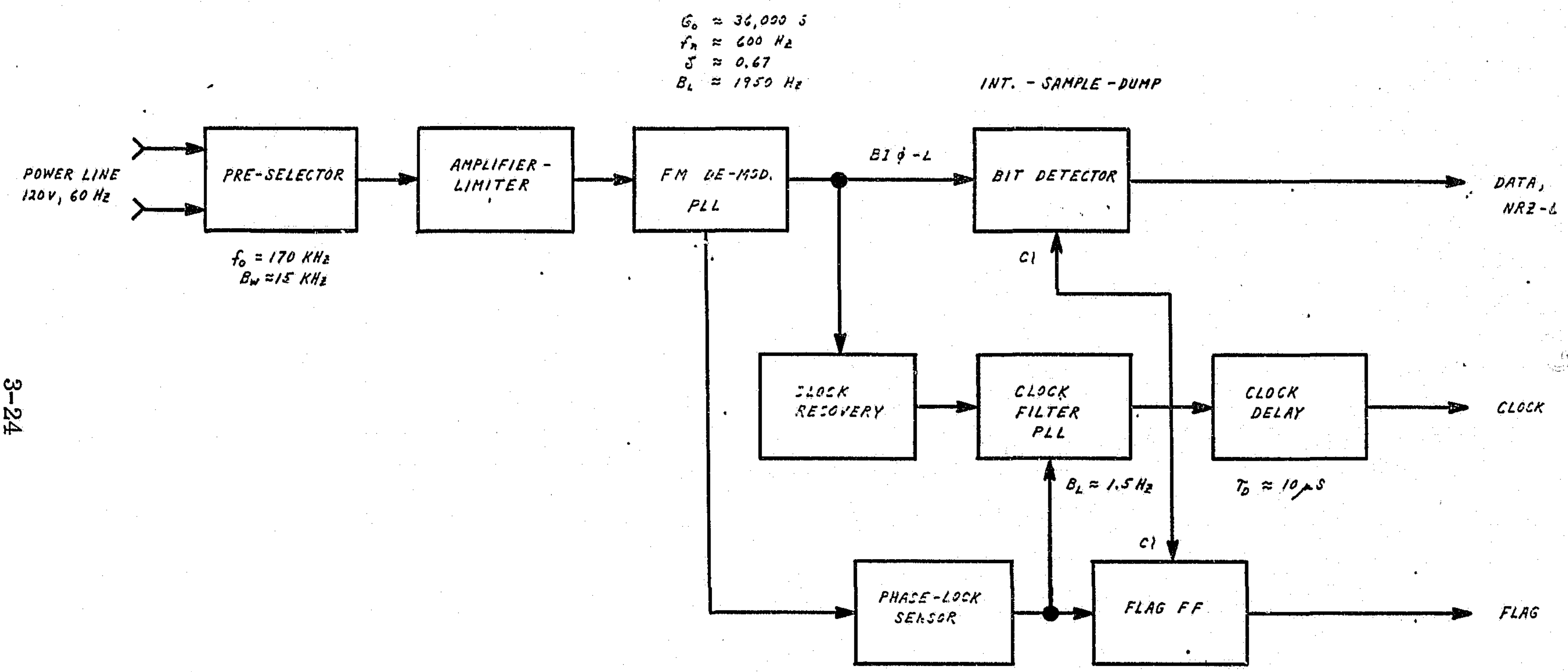

Figure 3-8. BAS Receiver Block Diagram

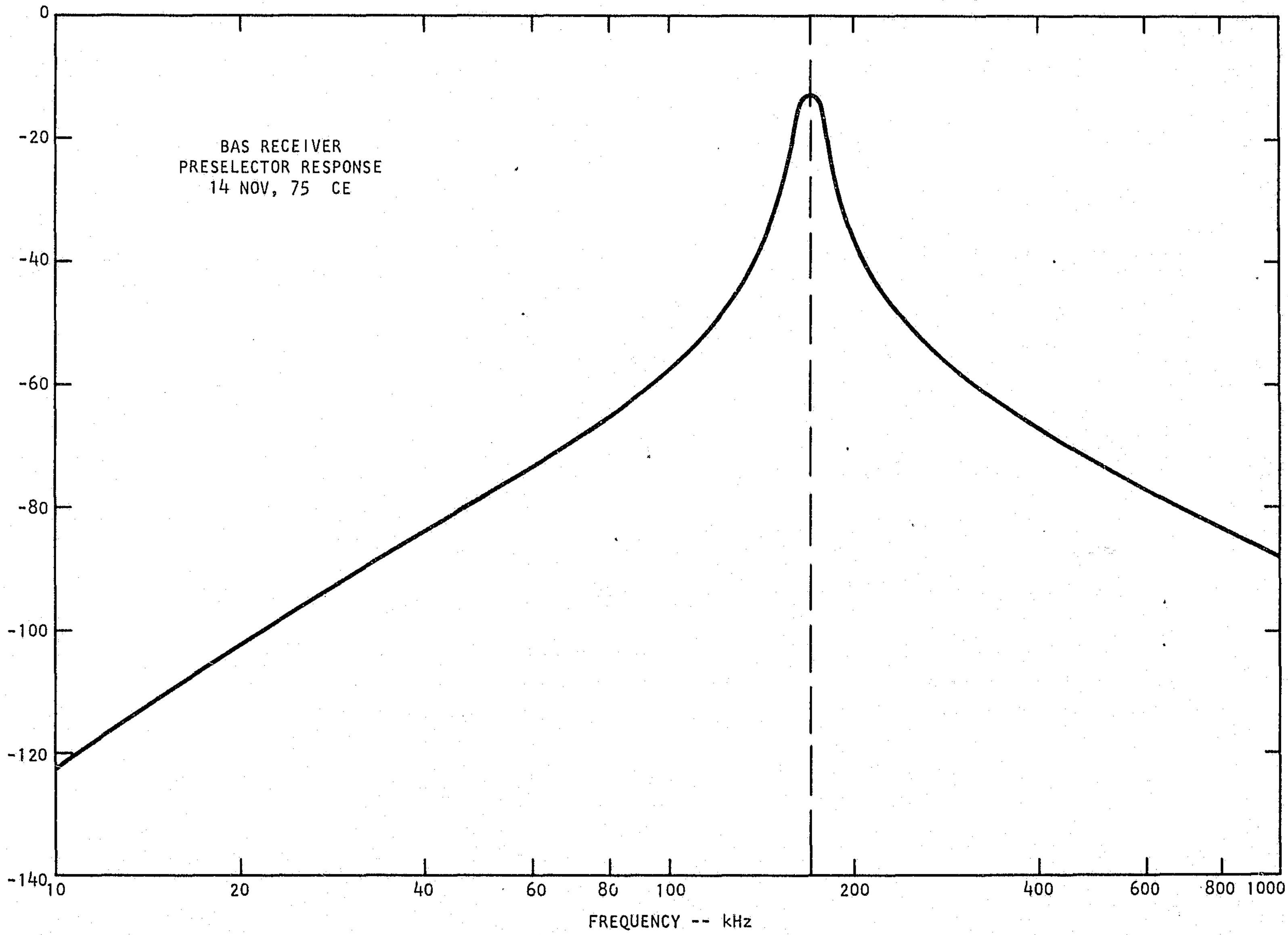

Figure 3-9. Overall BAS Receiver Preselector Frequency Response

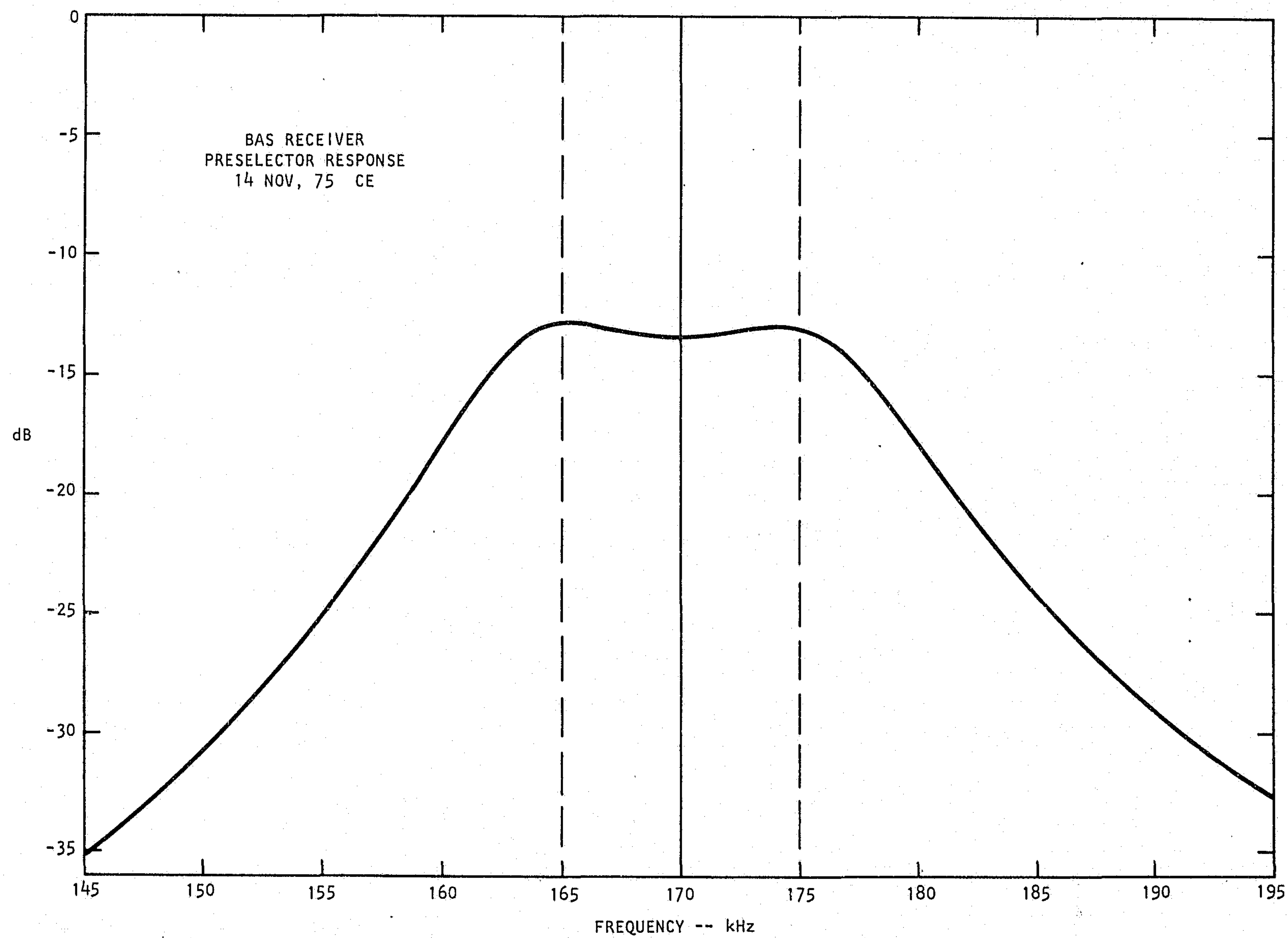

Figure 3-10. Enlarged Receiver Preselector Frequency Response Around 170 kHz.

3.2.2.3 (Continued)

Clock recovery is performed in two steps. In the first, a raw clock pulse is generated from each data bit midpoint transition (the output waveform from the FM discriminator is biphase level (BIΦ - L). The raw clock is not directly useful because it jitters when the discriminator output signal-to-noise ratio is low. In the second step, the raw clock jitter is reduced by a narrow bandwidth tracking filter. This filter consists of a phase locked loop, U6, with a switching circuit, U4, U5, to control the loop bandwidth. A practical difficulty with use of a tracking filter in a burst type data link is that the filter lock acquisition time is an inverse function of the loop bandwidth. If the bandwidth is narrow, appreciable time must be allowed at the beginning of each data burst for acquisition and some data may be lost. To circumvent this difficulty, the loop filter is removed until phase lock with the raw clock is achieved, and then it is connected to form a second order loop with narrow bandwidth. The switchover from first to second order filter is under control of a separate acquisition detector circuit using the number 2 phase detector of U6 with U4 and U5.

The bit detector converts the BIΦ - L wave from the FM discriminator to a NRZ output wave which is a replica of the transmitter encoder output. It uses an integrate, sample, and dump circuit to accomplish this. The circuit is shown at the bottom of the schematic diagram. U11B and U13, under clock control, switch the polarity of the BIΦ - L wave twice each bit period. The switch timing is such that the current integrating capacitor C30 does not reverse during a bit period. The output of comparator U14 is sampled in U15A by the leading edge of the clock. The output of U15A is the recovered NRZ data wave. U12D and U12C form a 10 microsecond clock delay circuit to ensure that receiver clock output transitions always follow data output transitions.

3.2.2.4 Communication Interface

The purpose of the communication interface is to input and output serial data for the microprocessor, with the power line receiver and transmitter and the telephone line modem. This is accomplished with a CD4034 universal shift register and a DG190 and a DG201 which are used for switching. A schematic diagram for this interface is also shown on SK00-3421 in Appendix A.

The DG190 switches the inputs from the RCVR clock to XTR clock and provides outputs on lins 1 and 3 to D6 on the data buss. It also switches the input from modem data to RCVR data and provides outputs on pins 6 and 8 to the input of the CD4034.

3.2.2.4 (Continued)

Phase lock indication is input to D7 on the data buss to tell the microprocessor that the receiver is receiving data, otherwise the normal position for the switches are in the position to receive data from the modem.

The DG201 switches the outputs from the CD4034 via AR1 for level shifting to either the XTR or the modem. The XTR is turned on by output D0 on U5. The modem is turned on by D1 on U5.

3.2.2.5 Code Plug Board

The code plug board in the Central Processor allows the user to establish the unique identity of his entire system, the "type" of his sensor transmitters (doors/windows, internal, fire, special, etc.) and his four-digit combination which is the "key" to the entire system. This combination is used at both the entrance control and the processor to arm/disarm the system, gain entry to the premises, change operating modes, etc. The code plugs "set" certain bits in the digital FSK messages transmitted within the system to provide the above functions. A photograph of the board is shown in Figure 3-11 and a schematic diagram is given in Appendix A as SK00-3420.

The code plug board consists of 20 IC packages, each of which are identical and bear the part number TID 121. This IC is composed of eight discrete diodes with their common cathode connected to pin 15. The anode pin is clipped off selectively to establish a high voltage (logical one) for that particular bit or if it is not clipped off then it is a low voltage (logical zero). A high voltage must be greater than 2.0 volts and a low voltage must be less than .85 volt.

Two of the code plugs are used to establish the user ID and two of them are used to determine the system combination.

The system combination may be set to any hexidecimal value from 0 through B inclusive, where the * sign on the keyboard corresponds to hexidecimal A and the # sign corresponds to hexidecimal B. Code plug U2 is used to establish digits 1 and 2, where D0 through D3 inclusive determine digit 2 with D0 as the least significant bit, and D4 through D7 inclusive determine digit 1 with D4 as the least significant bit. Code plug U1 is used to establish digits 3 and 4, where D0 through D3 inclusive

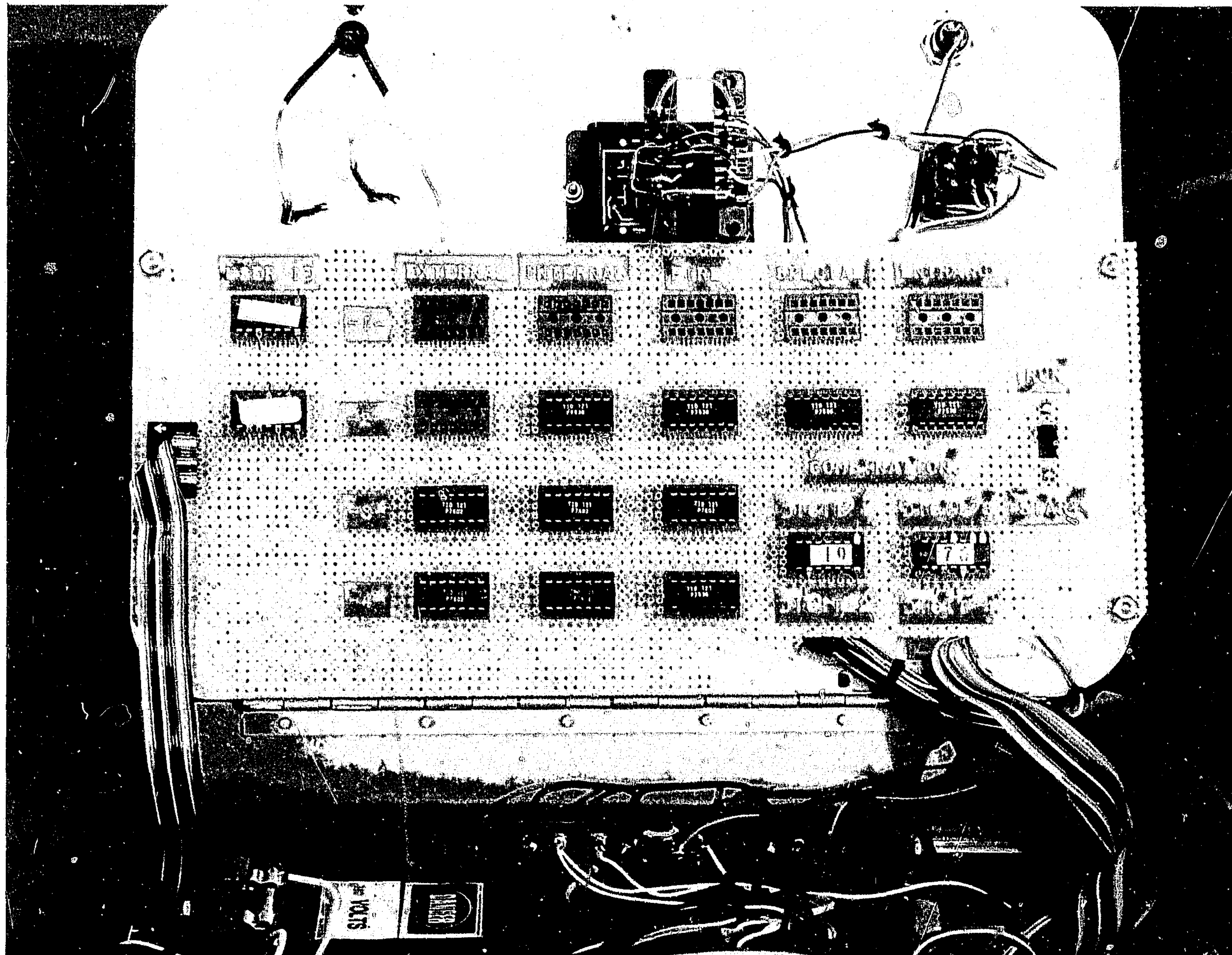

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Figure 3-11. Central Processor Code Plug Board

3.2.2.5 (Continued)

determine digit 4 with D0 as the least significant bit, and D4 through D7 inclusive determine digit 3 with D4 as the least significant bit. Digit 1 is the first digit depressed at the keyboard when entering the system combination.

Table 3-2. The Setting of Two Four-Digit Combinations (1976 and 2 * # 4) Using U2 and U1 Code Plugs

IC	U2								U1							
Pin	12	11	9	8	7	5	3	2	12	11	9	8	7	5	3	2
Bit	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Digit	1				2				3				4			

Example A

Combination	1				9				7				6			
Binary	0	0	0	1	1	0	0	1	0	1	1	1	0	1	1	0

Example B

Combination	2				*				#				4			
Binary	0	0	1	0	1	0	1	0	1	0	1	1	0	1	0	0

As shown in example A the combination "1976" is established in the processor by clipping or bending pins 2, 7, and 8 of U2 and 3, 5, 8, 9, and 11 of U1 to open them from the circuit.

In example B combination 2 * # 4 would be established by opening pins 3, 7, and 9 of U2, and pins 5, 8, 9, and 12 of U1.

The user ID #1 and #2 may be set in a similar manner, however, the actual decimal representation is unimportant. The only really important thing to know about the user ID is that all user ID code plugs in a system must have the same pins clipped off. The user ID allows the central processor to determine which messages it will receive and subsequently process.

The sensor/transmitter code plugs are removed from the code plug board and installed in the sensor/transmitter when that sensor/transmitter is entered into the system. This action tells the central processor that it should be receiving messages from this sensor/transmitter and also tells the sensor/transmitter what type of sensor/

3.2.2.5 (Continued)

transmitter it is so that it may appropriately encode its messages. The codes for these code plugs are shown in Table 3-3. All binary ones in the code indicate that the corresponding IC pin number shown at the top of the table should be clipped off.

Table 3-3. Code Structure for Sensor/Transmitter and Entrance Control Code Plugs

Code Plug Name	Hex Code	Code Plug Codes / Binary Code: Pin Bit	12 D7	11 D6	9 D5	8 D4	7 D3	5 D2	3 D1	2 D0
External #1	40		0	1	0	0	0	0	0	0
External #2	41		0	1	0	0	0	0	0	1
External #3	42		0	1	0	0	0	0	1	0
External #4	43		0	1	0	0	0	0	1	1
Internal #1	50		0	1	0	1	0	0	0	0
Internal #2	51		0	1	0	1	0	0	0	1
Internal #3	52		0	1	0	1	0	0	1	0
Internal #4	53		0	1	0	1	0	0	1	1
Fire #1	60		0	1	1	0	0	0	0	0
Fire #2	61		0	1	1	0	0	0	0	1
Fire #3	62		0	1	1	0	0	0	1	0
Fire #4	63		0	1	1	0	0	0	1	1
Special #1	70		0	1	1	1	0	0	0	0
Special #2	71		0	1	1	1	0	0	0	1
Entrance #1	80		1	0	0	0	0	0	0	0
Entrance #2	81		1	0	0	0	0	0	0	1

In the delivered systems only the code plugs listed above were installed, however, the number of bits available on the code plug allow for the coding of up to 16 of each type of sensor.

3.2.2.6 Front Panel

The front panel of the Central Processor is shown in Figure 3-12 and a schematic diagram is shown in Appendix A as SK00-3419. There are two LEDs at the top of the front panel. The one at the upper left when lit, indicates that the system is armed. The one at the upper right indicates that the system is in the access mode when lit. When in the access mode the front panel may be opened to gain access to the code plugs and change the system combination. The access mode also allows the sensor mode and alarm mode to be changed. The sensor mode and alarm mode are rotary switches and are located at the right hand side of the front panel. The position of these switches are only read into the microprocessor while in the access mode of operation. The LEDs located at each of the switch positions light up to indicate the set modes of operation when in the access mode or when the "Illuminate Trouble Indicator" button is depressed. This is necessary since the switch position may be changed while the system is not in the access mode and then the switch position and mode of operation would not be the same. The "Illuminate Trouble Indicator" button also causes the two-digit decimal display to light with a code that indicates the status of the system. If there is more than one trouble in the system the additional codes may be viewed by additional depressions of the switch until the codes begin to repeat. The trouble codes will be displayed in the same order in which they occurred. The codes are explained in the software section of this report and are also taped to the inside of the lid of the Central Processor. The local alert is a buzzer located at the bottom center of the front panel and emits a beeping tone for a fire and a steady tone for all other alarms except when in the remote alarm mode of operation.

The keyboard is located at the lower left hand corner of the front panel and is used to enter the system combination to place the system in the access mode or to terminate or abort a system arming operation. This combination is the same four-digit code used at the entrance control to gain entry to the premises.

The schematic for the front panel is number SK00-3419 as given in Appendix A. As can be seen from the schematic all switch inputs from the front panel merely place a ground on the appropriate bit. The outputs also provide grounds to the lights or local alert to turn them on.

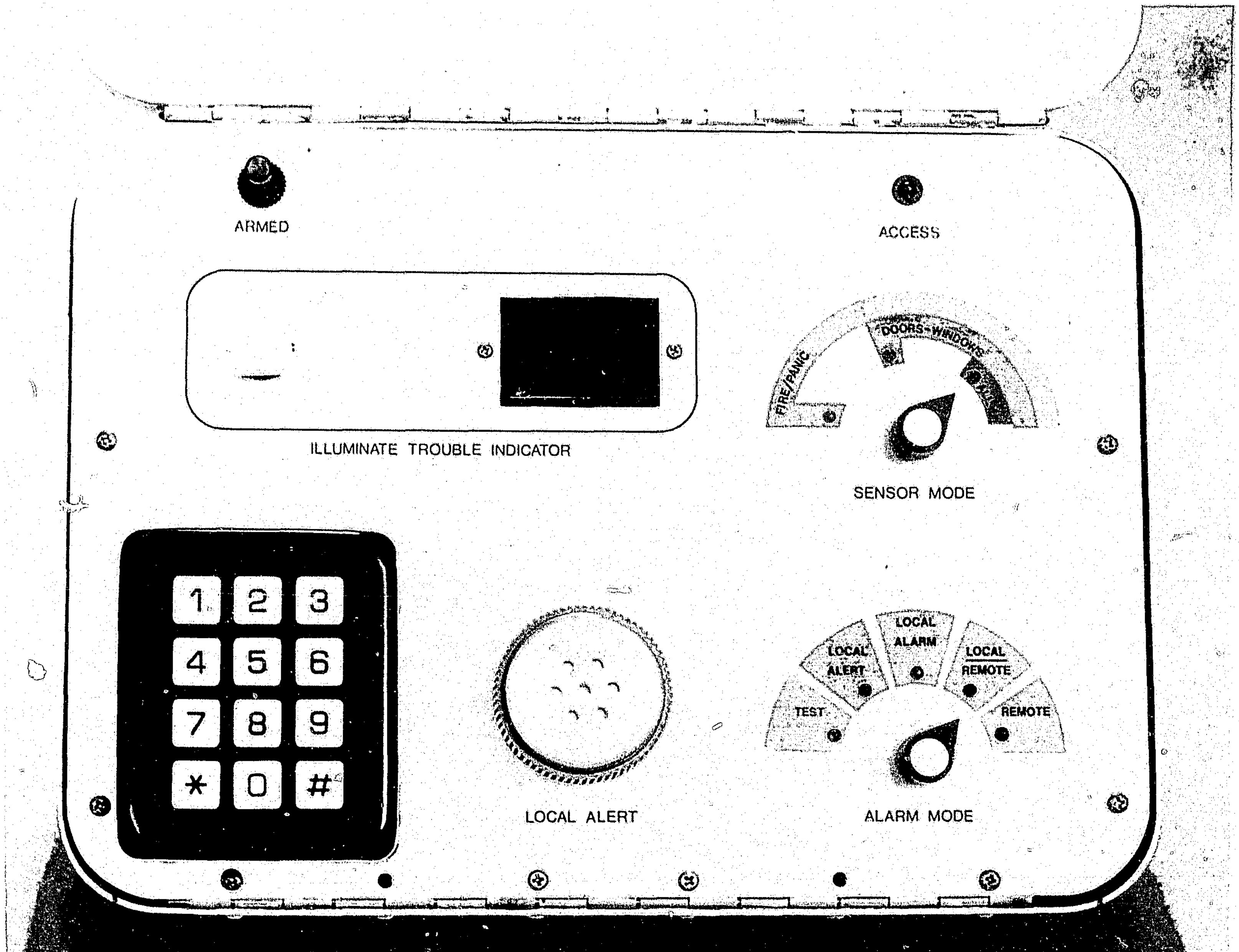

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Figure 3-12. Central Processor Front Panel

3.2.2.7 Power Supply

Dynamic Measurements Corporation Power Supply Model 4630 is used to convert 117 VAC to +12, -12, and +5 VDC. The -12 VDC output is used to generate -5 VDC. The power supply schematic, SK00-3424 in Appendix A also shows the circuits used to drive the external alarm bell and the strike release at the entrance control. The strike release circuitry is only included in the power supply circuitry associated with the entrance control and is located in the auxilliary electronics box. The bell driver circuitry is located only in the central processor. The Dynamic Measurements Corporation power supply is not field maintainable. This power supply is used in the central processor, the entrance control auxilliary electronics box, and in the central station. The variety of voltages are required to drive the INTEL 8080A.

In a production system a single voltage microprocessor would be used which would radically simplify the power supply requirements and subsequently minimize cost.

Figure 3-13 shows the power supply as installed in the central processor box. Figures 3-17 and 3-29 show the power supply installed in the auxilliary electronics box and the central station respectively.

3.2.3 Central Processor Mechanical Description

The front panel of the central processor was intended to represent the final version which would be used in the production phase. The panel was human engineered to simplify the functional operations and make it aesthetically appealing. For reasons of economy in production, it would be molded in plastic as an integral part of the housing. However, for the two deliverable breadboard models, aluminum was used and a triple anodize technique employed for adding color and durability. Anodizing adds a hard, marproof finish which is considered essential for demonstration systems. Actually, a molded plastic panel with the colors and nomenclature hot stamped is just as durable; but again, tooling cost for only two panels is quite prohibitive.

A mechanical layout of the central processor is shown in Figure 3-14. The case, which is a deep-drawn aluminum can, was selected after all the electrical components and assemblies were identified. The combinations of wire-wrap and printed circuit boards plus other large components dictated the final size. Initially, a double hinge approach was used on the case cover and front panel but proved somewhat less than desirable; again because of additional tooling.

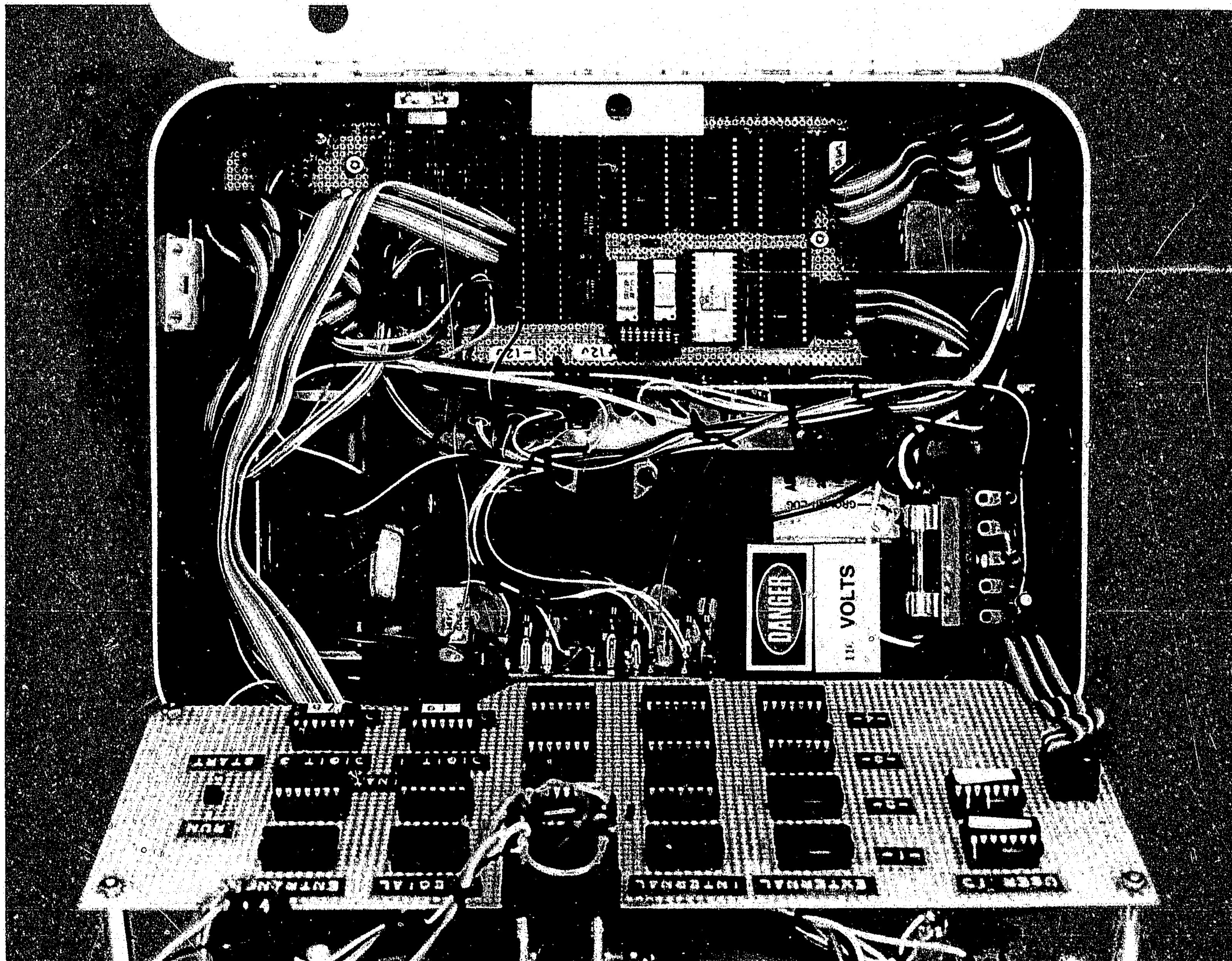

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Figure 3-13. Internal View of Central Processor

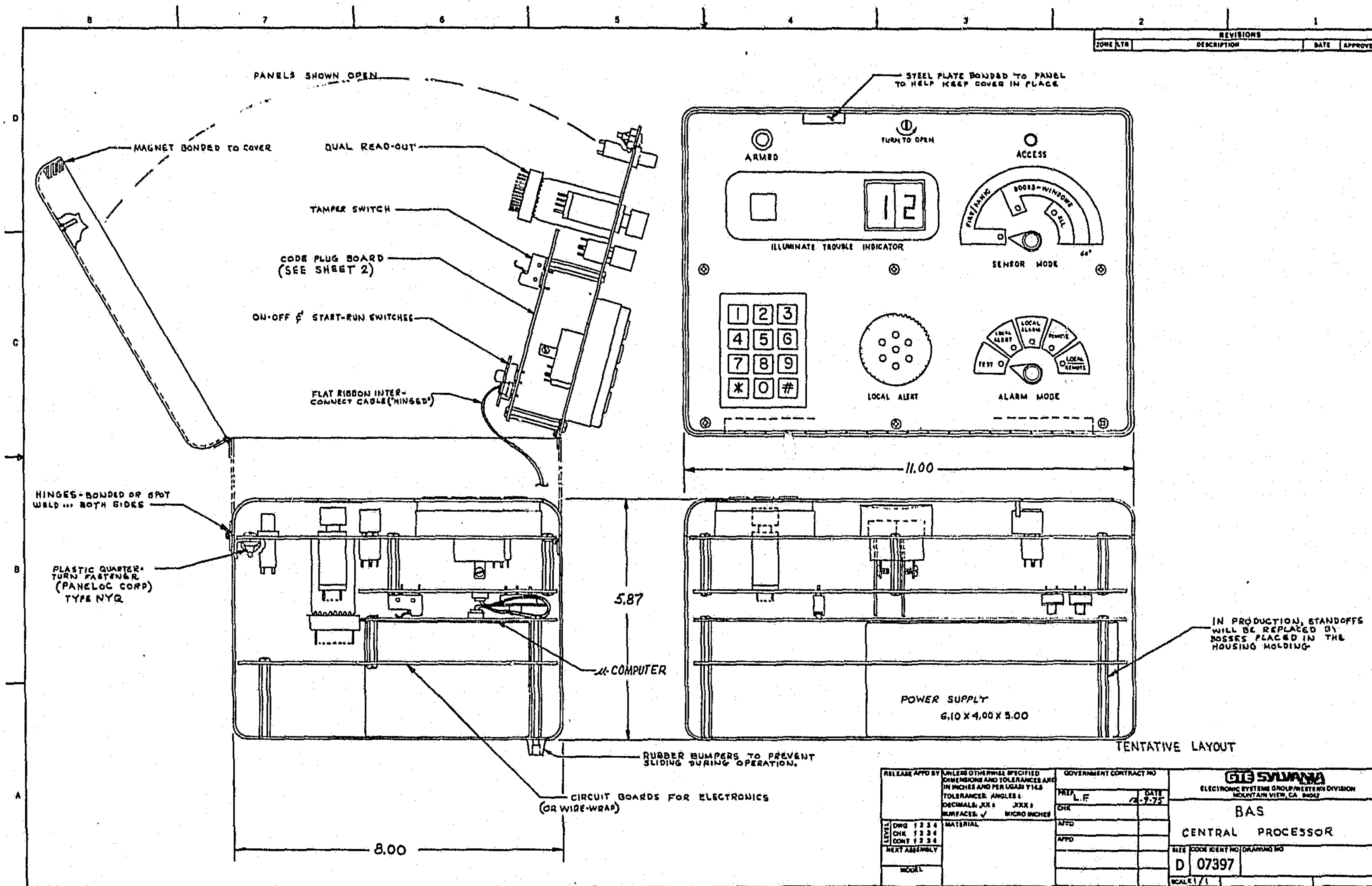

Figure 3-14. Central Processor Mechanical Assembly

3.2.3 (Continued)

A special hinge was required which was unavailable. An attempt was made to design around standard hinges (which was difficult) but represented, in part, the final concept which was proposed to be employed in the production phase.

Because of having to design around standard size components, the central processor housing was about three times deeper than that which would be used in production. A smaller, more "modern" case would evolve with the advent of miniaturized circuit components, (e.g., LSI, MSI, thick-film hybrid, etc.) along with the use of injection molding techniques or a similar process.

3.3 ENTRANCE CONTROL

3.3.1 Functional Description

The purpose of the entrance control is to prevent user caused false alarms, i.e., a user walking into an armed system. This is accomplished by providing the user with a keyboard located on the exterior of the premises and an electric strike and associated electronics on the interior. The same four-digit combination set at the central processor is used to gain entry. The entrance control further encodes the combination data, transmits it over the power line and if the central processor recognizes it as a valid combination it will disarm the system and transmit a "strike release" signal back to the entrance control to provide entry to the user. The entrance control also alerts the user of trouble in the system whenever the system is armed at the entrance control and whenever the user reenters. This is done via a LED located on the keyboard. If the LED glows continuously for 20 seconds all conditions within the system are fine, however, if the LED pulsates for 20 seconds then this indicates trouble in the system. The user may then go to the central processor to press the "Illuminate" button and the user will be notified of specific troubles in the system via two-dit codes which will be illuminated on the LED display. The entrance control also provides a door position sensor, panic buttons and tamper protection. A block diagram of the entrance control is shown in Figure 3-15 and a photograph of the hardware is shown in Figure 3-16.

The entrance control also contains a microprocessor whose primary function is to encode data and communicate over the power line to the central processor. All data is input through one input port in an identical manner to the central processor,

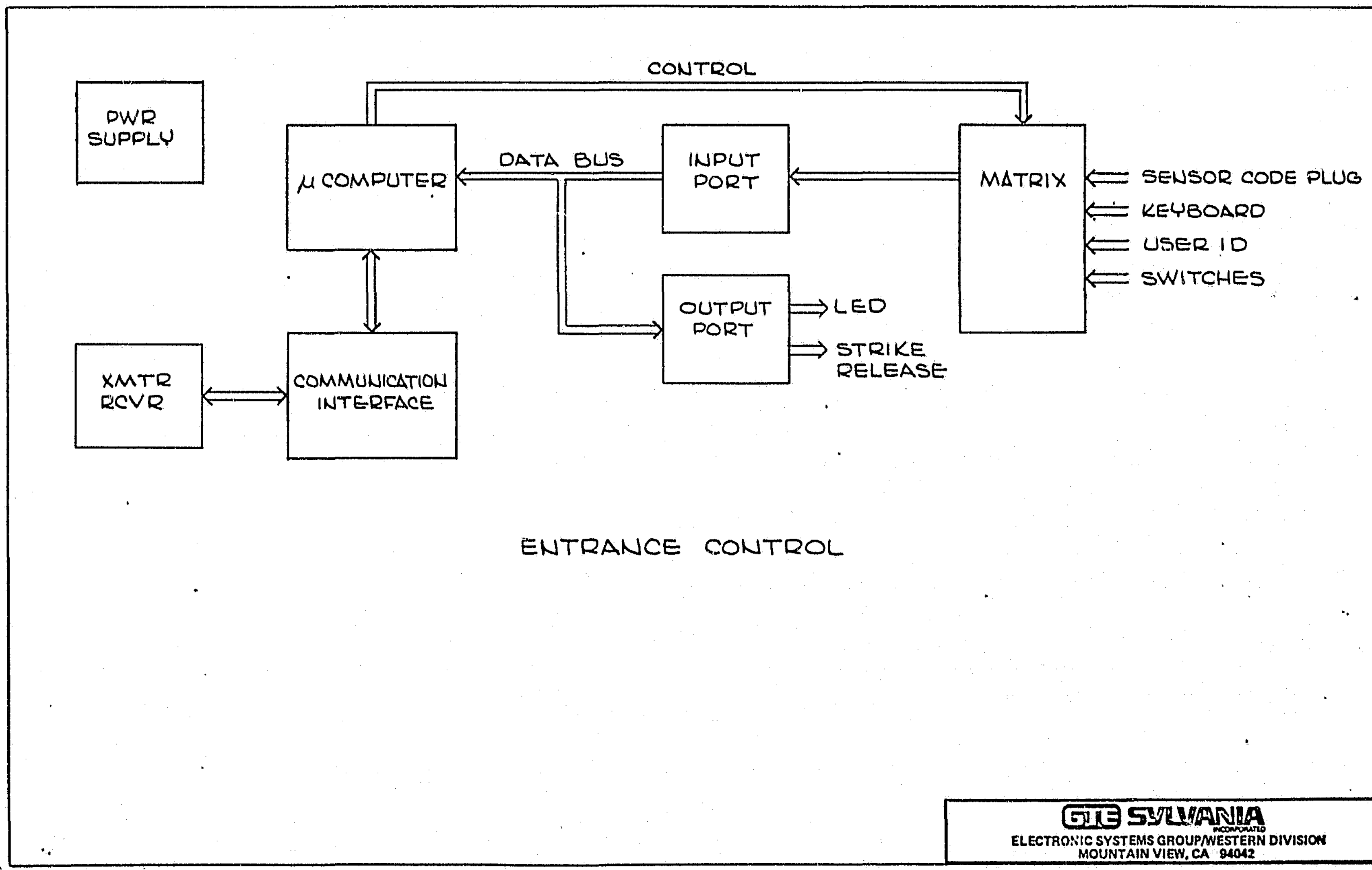

Figure 3-15. Entrance Control Block Diagram

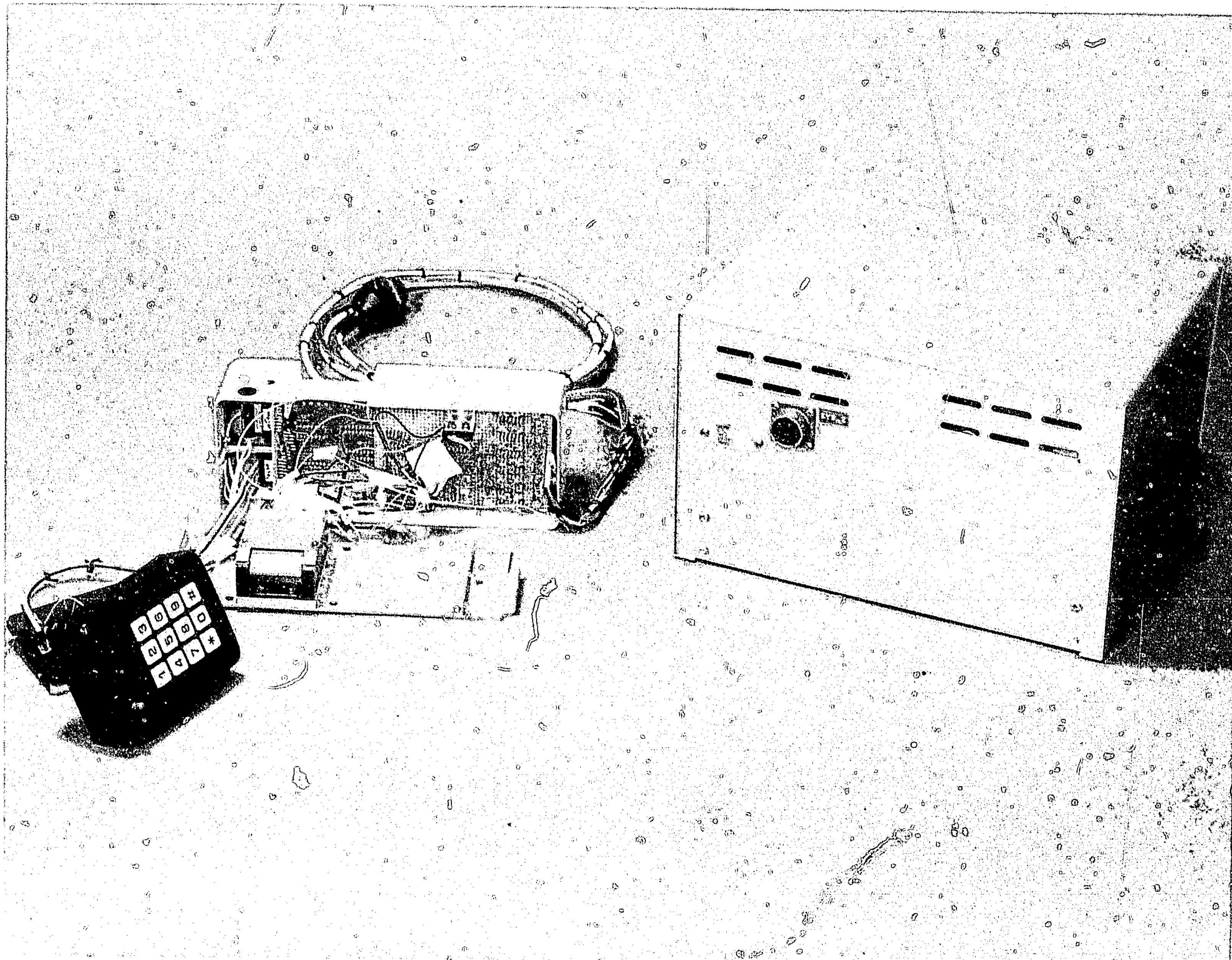

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Figure 3-16. Entrance Control Hardware

3.3.1 (Continued)

the data input is the 16 bit user ID, the 8 bit sensor code plug, the 12 keys of the keyboard, and the tamper, arm, panic, and door sense switches. Only one output port is used at the entrance control to control the electric strike driver, and the LED which is used to indicate that there has been trouble in the system by flashing after releasing the strike. The LED comes on steady for 20 seconds when the system is being armed.

The communication interface is used as a bidirectional I/O port to transmit and receive data, over the power line.

The microprocessor and I/O circuitry shown on schematics SK00-3415 and SK00-3422, located in Appendix A, are in the housing installed on the door. The power supplies, strike release driver and transmitter/receiver are installed in the auxilliary electronics box.

In a production system, miniaturization would allow for all of the electronics to be located in the housing installed on the door.

3.3.2 Circuit Description

3.3.2.1 Microprocessor

The microprocessor installed in the entrance control is identical to that in the central processor (discussed in Section 3.2.2.1) with the exception that U9 (a 1KX8 bit PROM) was not required due to a smaller software program. The schematic for the microprocessor board is given in SK00-3415 in Appendix A.

3.3.2.2 I/O Matrix

The entrance control I/O circuitry is essentially identical to the central processor (discussed in Section 3.2.2.2) except that it has fewer inputs and outputs. It has the same keyboard, and user ID inputs. It inputs all 8 bits of the sensor code plug, and inputs four switch positions, the tamper, arm, door sense, and panic switches. The output port is only used to control the strike release, and the trouble indicator LED on the keyboard. The schematic is shown in SK00-3422 in Appendix A.

3.3.2.3 Communication Interface

The communication interface is the same at the entrance control as it is at the central processor (discussed in Section 3.2.2.4) with the exception that there is no modem to receive data from or transmit to so there is no DG201 in this circuit to switch for the level shifting required in the central processor. The schematic is given in Appendix A as SK00-3422).

3.3.2.4 Auxilliary Electronics

The auxilliary electronics box contains the receiver, transmitter, strike release power supply and microprocessor power supply for the entrance control. In a production effort this circuitry would be simplified and miniaturized to enable it to be installed in the entrance control on the door. A photograph of the inside of the unit is shown in Figure 3-17. The receiver and transmitter are discussed in detail in Sections 3.2.2.3 and 3.4.2.1 respectively.

3.3.2.4.1 Strike Release

The strike release power supply is shown in schematic SK00-3424 of Appendix A. It converts 117 VAC to 4V with a drive capability of 1-5A, which is turned on by the input of R14.

3.3.2.4.2 Microprocessor Power Supply

The entrance control power supply is identical to the central processor power supply with the exception that the bell driver is only installed in the central processor. The power supply was previously discussed in Section 3.2.2.7 and the schematic is given as SK00-3424 in Appendix A.

3.3.3 Entrance Control Mechanical Design

From a mechanical standpoint, the entrance control was probably the most difficult piece of BAS equipment to design. This is because of the great variations in door jamb configurations from house to house, house to apartment, and house to commercial establishments. (See recommendations at the end of this section). Trying to develop a universal control to fit every application, with the condition that it be installed by the home owner is a real challenge. The problem would be reduced significantly by the use of ultraminiature components encased in a small plastic housing. However, even with electronic miniaturization techniques, the electric strike cannot be reduced much in size over the one presently being used without sacrificing the mechanical strength needed to prevent a forced entry (e.g., shoulder against the door, etc.).

The breadboard entrance control was designed around standard discrete components which were packaged on printed circuit and wire srap boards. The size of the case was dictated by the circuit cards and the electric strike. A mechanical drawing of

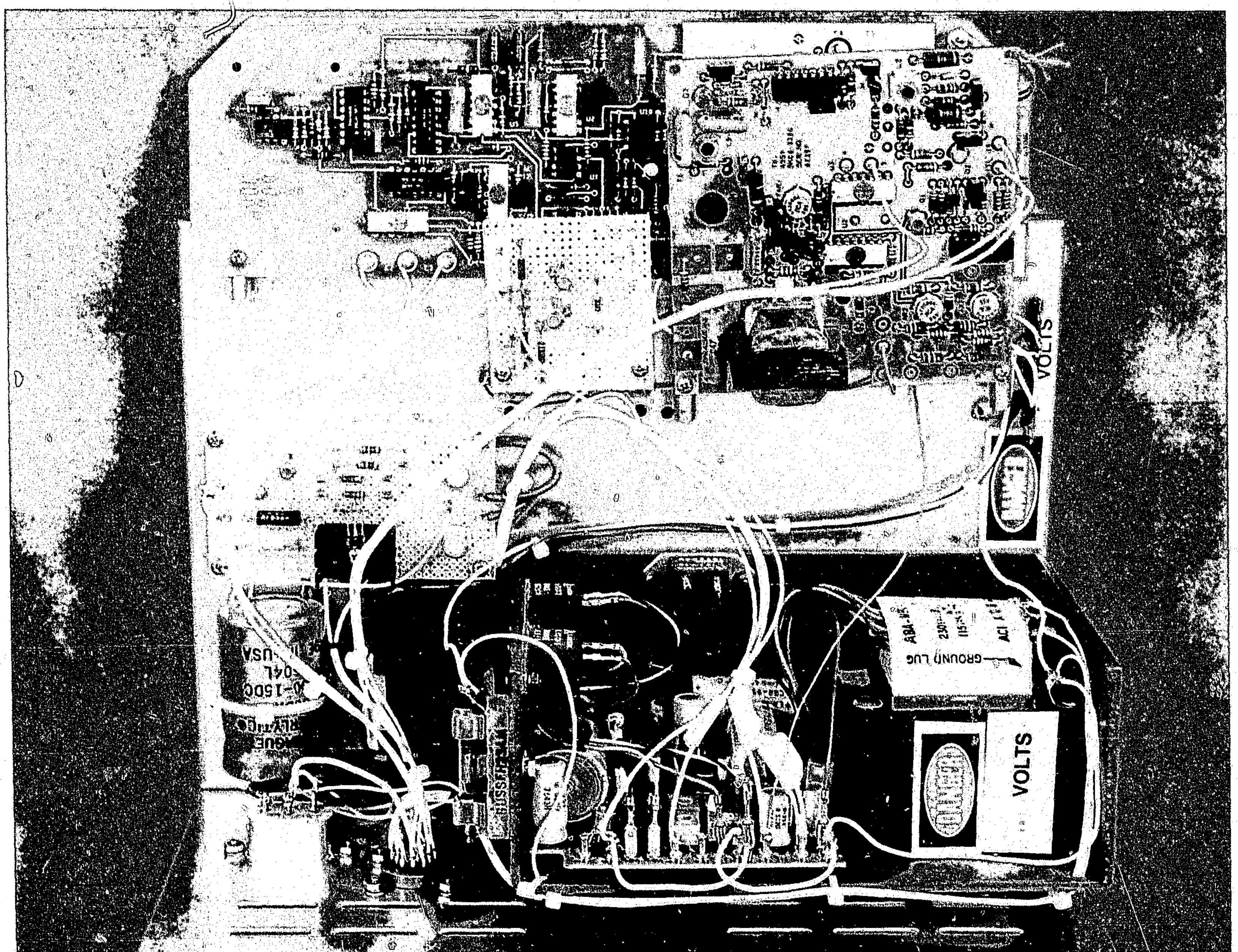

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Figure 3-17. Entrance Control Auxiliary Electronics

3.3.3 (Continued)

the electronics/strike release housing is shown in Figure 3-18. A deep drawn can was used for the housing to eliminate sharp edges and corners. The relatively heavy base plate was designed to add support for the electric strike. In order to provide a more positive protection against intrusion, the base must be securely attached to the door jamb.

The door latch was packaged into a separate housing to mate with the electric strike and to provide room for the magnet part of the door sense switch. This assembly is shown in Figure 3-19. In production the magnet would be provided as an integral part of the latch by the manufacturer.

The outside keyboard shown in Figure 3-20 is straightforward in the mechanical design approach. In production, the small metal frame that was used would be a part of the keyboard housing.

For future considerations, the electric strike should be changed to a jamb-type mount. This would make the entrance control much smaller and eliminate the surface mounted night latch; allowing the user to use the existing door lock. Because a mounting template would be provided with a BAS, this configuration would probably not be much more difficult to install. Right or left hand door openings would not be a problem - nor would the small aluminum store door frames.

3.4 SENSOR TRANSMITTERS

3.4.1 Functional Description

The function of the sensor transmitters is to generate modulated radio frequency signals (secure, alarm, and status messages) for transmission to the system receivers by way of the power line. Remote sensor transmitters respond to sensor switch operation by generating a 0.67 second RF burst which is frequency modulated by the encoder message. The burst is repeated at one minute intervals until five identical messages have been transmitted. In addition, if an alarm or secure message has not been sent during the preceding hour, the transmitter generates a status message to indicate that it still functions. Transmitters associated with the central processor and entrance control do not contain encoders. Instead, they generate messages encoded by the logic circuits of the host unit. A photograph of a sensor transmitter is shown in Figures 3-21 and a block diagram is shown on Figure 3-22.

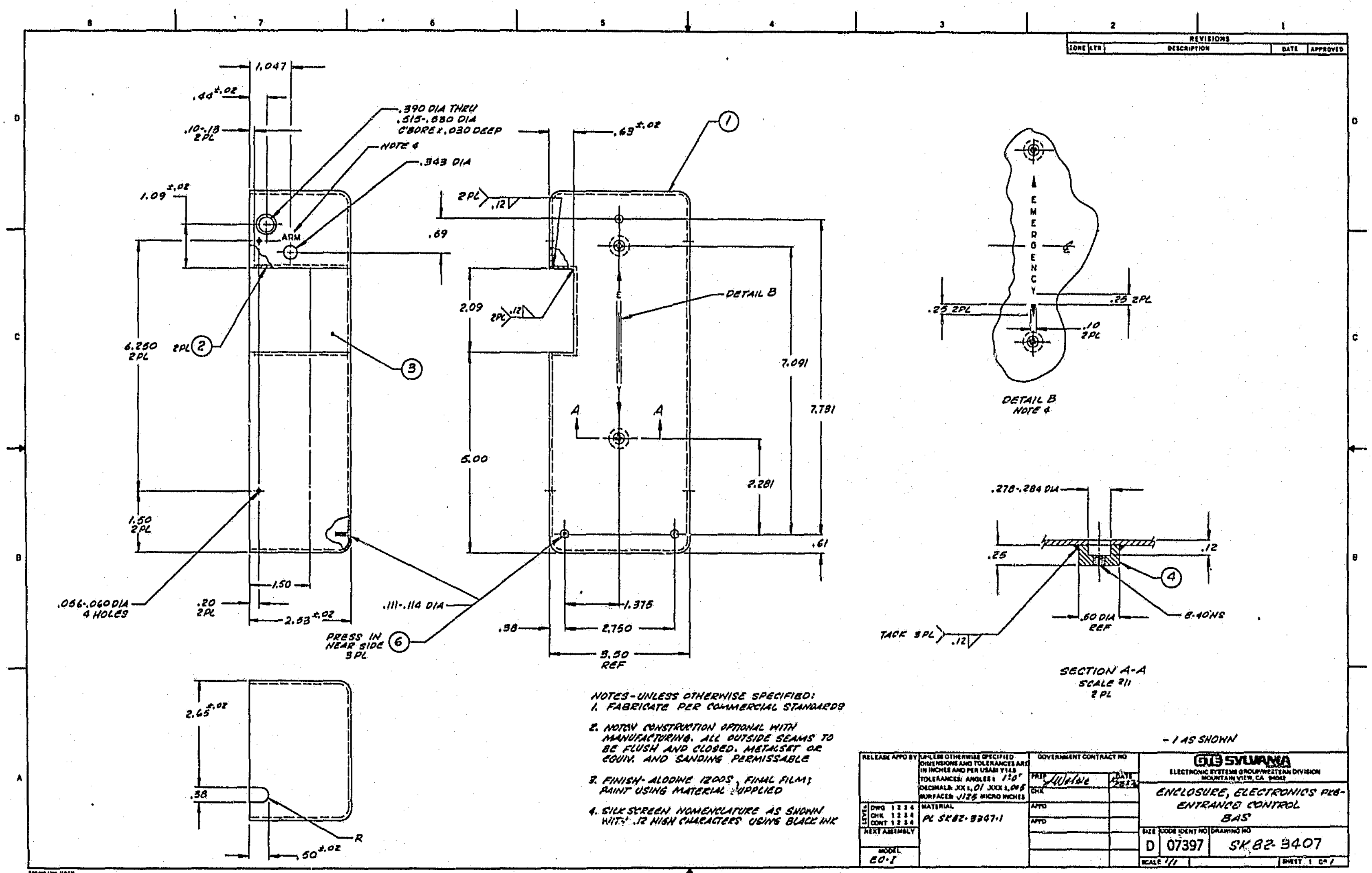

Figure 3-18. Entrance Control Electronics Mechanical Assembly

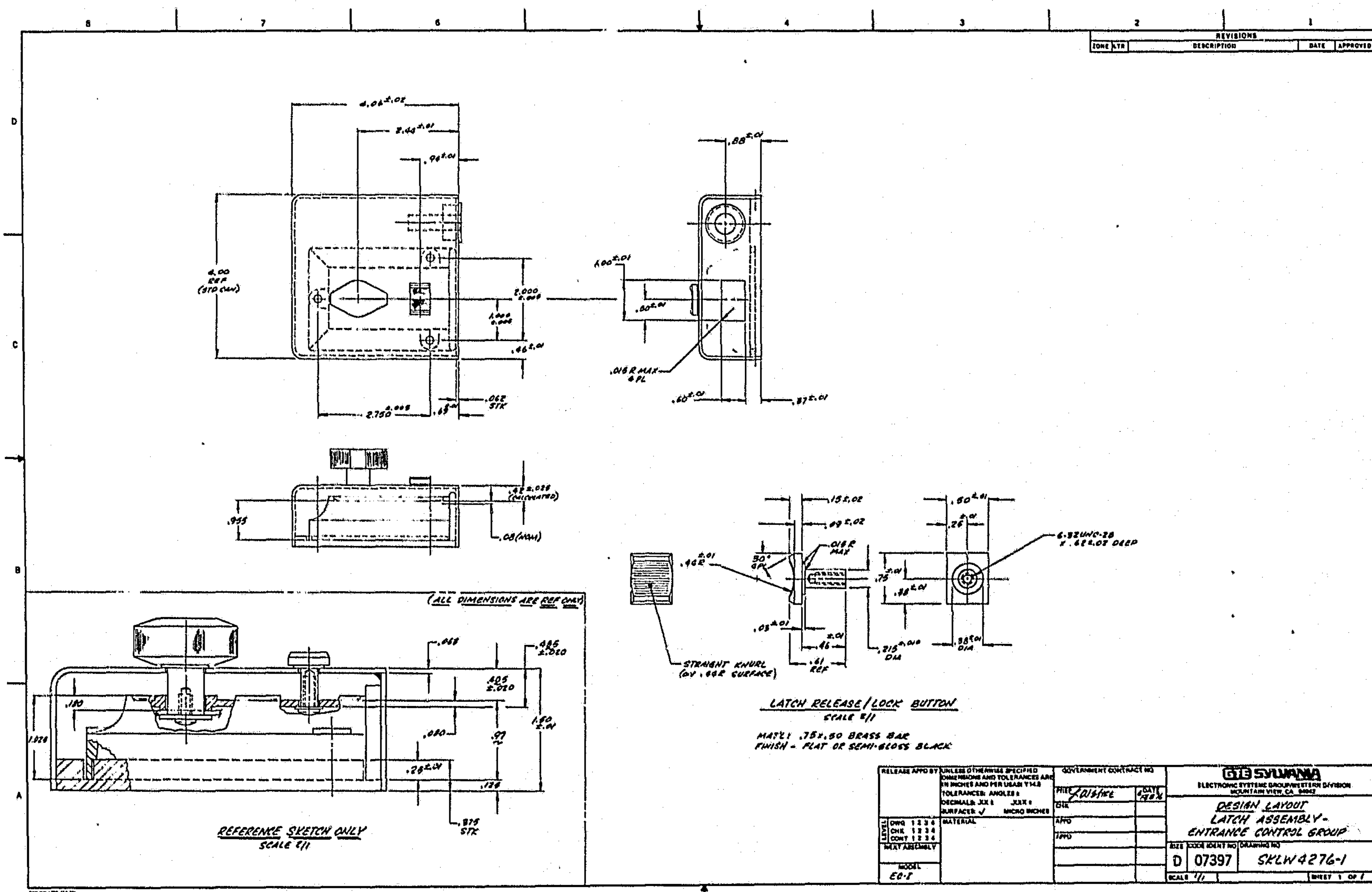

Figure 3-19. Entrance Control Latch Assembly

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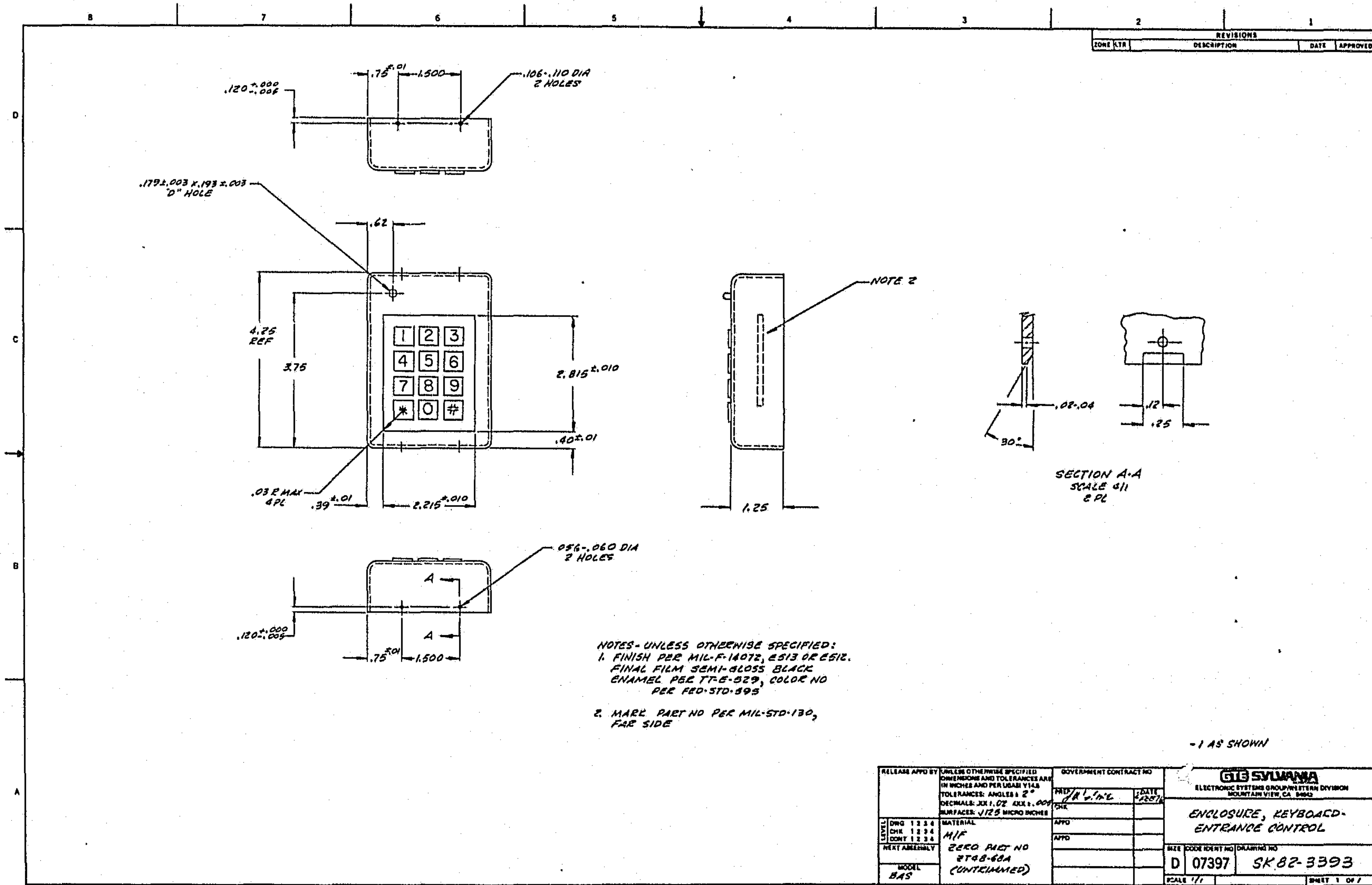

Figure 3-20. Entrance Control Keyboard Assembly

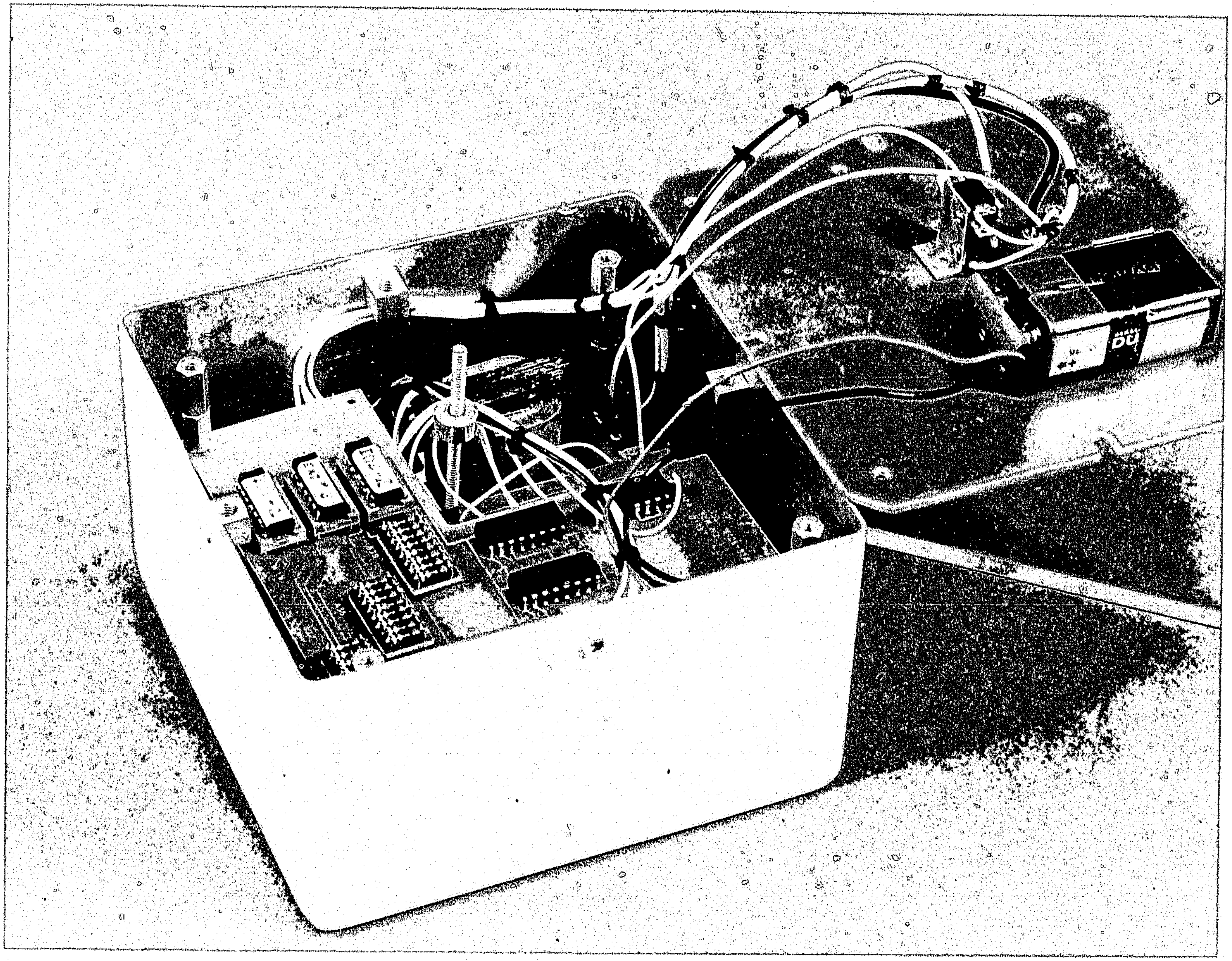

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Figure 3-21. Sensor-Transmitter

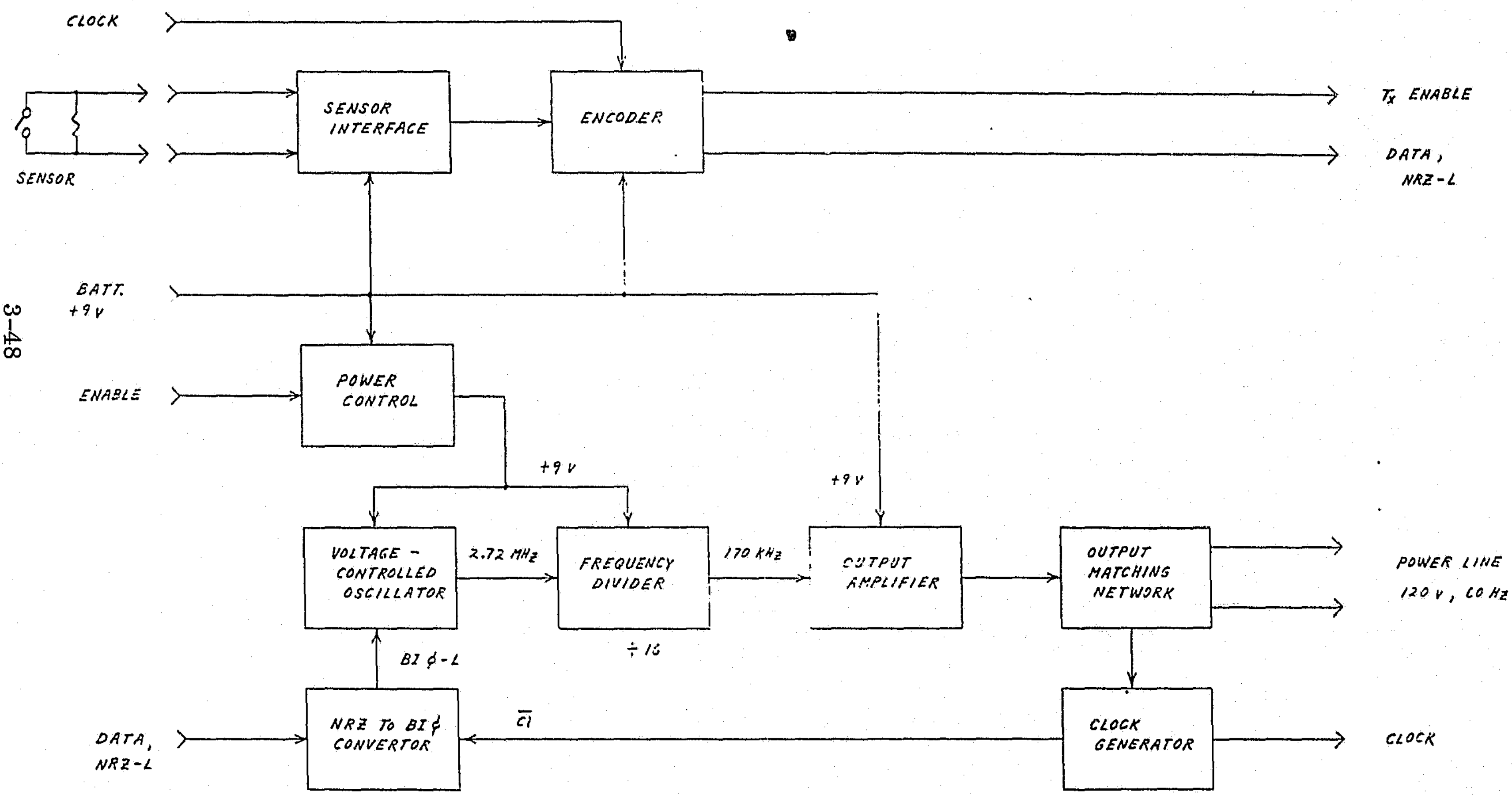

Figure 3-22. Sensor Transmitter Block Diagram

3.4.1 (Continued)

The sensor interface circuit detects either a short circuit or an open circuit at its input terminals. It may be wired via the terminal block to operate with either normally open or normally closed sensor switches. Continuity of the leads to the sensor switch is monitored. If the leads are cut an alarm message is generated.

A sensor switch actuation causes the encoder to receive a voltage level shift from the sensor interface circuit. In response, the encoder generates a serial digital message to modulate the RF circuits. At the same time, a transmitter enable signal is generated to turn on power to the RF circuits. A 60 Hz clock signal is fed to the encoder continuously from the clock generator.

The message output of the encoder is in NRZ form which is not suitable for direct use in an RF link designed for burst operation. There are two reasons for this. First, it is difficult to establish the clock at the receiver because there may be only a few data bit transitions during the message interval. The second is that the receiver is required to have extended low frequency video response in order to reproduce NRZ waveforms. Therefore, the NRZ output of the encoder is converted to a biphase level (BIΦ - L) wave before it enters the modulator circuit of the transmitter. A BIΦ - L wave always has a voltage or current transition at the midpoint of each data bit. This waveform is easier to reproduce and utilize at the receiver. Clock can be recovered with simple circuits and extended low frequency response is not required in the video system. The data link timing diagram, Figure 3-23, shows a representative NRZ wave on line 1 with the corresponding BIΦ - L wave on line 3.

The radio frequency circuits of the transmitter consist of a voltage tuned oscillator, a frequency divider, an output amplifier, and a power line coupling network. The oscillator operates at 2.72 MHz, a convenient frequency permitting the use of small and inexpensive timing components. The frequency divider is a four stage ripple counter which drives the output amplifier at 170 kHz. The divider provides ocillator isolation and power amplification. The output amplifier supplies 50 milliwatts of power through the line coupler to an external 20 ohm load. The line coupler provides low frequency isolation from the power line and considerable attenuation of transmitter harmonic frequency output.

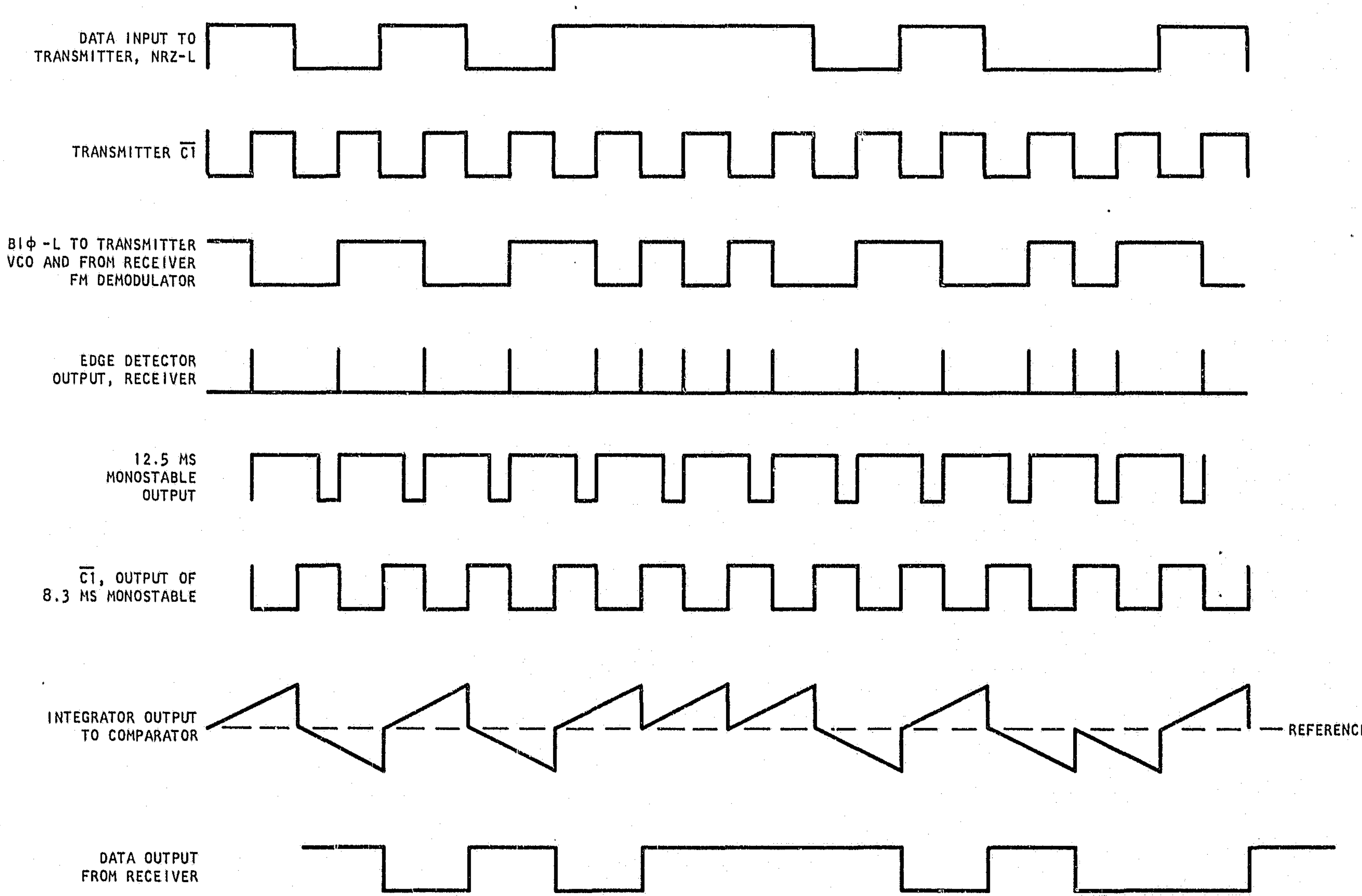

Figure 3-23. Data Link Timing

3.4.1 (Continued)

The sensor transmitters are operated from a small 9 volt battery. To conserve battery life, the power control circuit disconnects the high current circuits from the battery, except during burst generation. The power output stage is not disconnected because it does not draw battery current without RF excitation. The only continuously active circuits are the clock generator, the encoder counters, and the sensor interface. Transmitters associated with the central processor and the entrance control receive dc power from the host unit supplies.

3.4.2 Circuit Descriptions

The transmitter and encoder circuits will be described in the following two subsections.

3.4.2.1 Transmitter Circuit Description

Reference will be made to SK00-3381 in Appendix A which is the schematic diagram of the radio frequency and control circuits of the data link transmitters. The encoder is described separately in Section 3.4.2.2.

The sensor interface circuit is made up of a two-level voltage comparator using amplifiers AR2 and AR3, followed by a logic OR circuit using U2B and U1A. A low pass filter is inserted at the comparator input to reduce susceptibility to transients coupled into the sensor switch leads from power wiring. The TB1 allows the user to wire the interface to operate with either normally open or normally closed sensor switches. In either case, integrity of the wiring to the sensor switch is monitored. Low current circuitry is used to minimize battery drain.

Clock generator circuits are shown on the upper part of the diagram. U2A and U2D make up an astable 60 Hz oscillator which operates continuously. AR1 generates a square wave at the power line frequency. It is driven from the power line by way of T2 and the low pass filter R1, C1, R2, C2. The filter attenuator high frequency noise, which would cause clock jitter if it reached AR1. U3B, U3A, and U3D make up a selector switch that connects the clock output line to either the astable oscillator or to the line driven square wave generator. Selection is controlled by the dc bias to U2C, which is derived from the power line. If the line is energized, bias is present and the clock line is connected to AR1. If the line is not energized, the clock line is connected to the astable oscillator.

3.4.2.1 (Continued)

The NRZ data output of the encoder is converted to BIΦ - L by the EXCLUSIVE OR gate, U1D. The inputs to U1D are the data output of the encoder and the clock complement from inverter U3C.

The radio frequency circuits are shown on the lower part of the schematic diagram. The oscillator is of the LC type with voltage controlled varactor vernier tuning. A current limiting RF feedback circuit stabilizes the amplitude level so that predictable varactor operation is obtained. The digital input signal is coupled to the varactor with an amplitude limiting low-pass filter network. This network controls the frequency deviation of the oscillator and the sideband energy distribution. The oscillator may be set on frequency by adjustment of L2. The output amplifier is coupled to the oscillator by U4, a four stage ripple divider. The oscillator frequency is not affected by amplifier tuning or changes in loading because of the high degree of isolation provided by the frequency divider. Division by 16 was selected because this permits the oscillator to operate at a convenient frequency.

The transmitter output stage is driven by the 170 kHz square wave output of the frequency divider. A diode network limits the driving voltage so that the peak collector current of the amplifier may be controlled by the emitter series resistor. An important requirement is that the amplifier be stable under all operating conditions. The actual load impedance at the output terminals of the transmitter can vary from a short circuit to an open circuit, although its normal range is 10 to 50 ohms. Resistances are designed into the output network and line coupler so that the range of load impedance presented to the amplifier transistor, Q3, cannot exceed 8 to 1.

The RF circuits are turned on by a positive voltage level at the enable input. The oscillator and frequency divider are connected to the battery through Q1 and the oscillator starts up immediately.

3.4.2.2 Digital Encoder

The input signals to the transmitter encoder are the 60 Hz input and the conditioned sensor indication. The output signals are the (transmitter) enable and the serial output.

The description of this unit will be conducted with reference to the schematic diagram of the transmitter encoder, SK00-3385 given in Appendix A. In cases where multiple gates or flip-flops are contained in a single package, gate or flip-flop designations

3.4.2.2 (Continued)

will consist of the package designation followed by a letter depending on the magnitude of the pin numbers associated with a particular gate or flip-flop. The gate or flip-flop connected to pin 1 will have the suffix A, the circuit having the next lowest pin will have suffix B, etc. In cases where the gate or flip-flop is connected to non-consecutively numbered pins, only the pin having the smallest number will be considered in assigning suffixes.

The 60 Hz input is the basic timing signal of the unit. It is used as the clock signal for the output shift register (U24, 33, 36, 38, 40), the enable counter (U19), and the sensor synchronizers (U7A and B). Since it is necessary under some circumstances to produce outputs at minute and hour intervals, the 60 Hz input is divided down to produce minute and hour timing pulses. All circuitry is CD4000 series CMOS logic. The minute timing pulses are produced by a CD4020A 14-bit ripple counter and its associated decoder and reset circuits. Since there are 3600 cycles of the 60 Hz input in a minute, it is the purpose of the decoder to detect when state 3600 is reached. The required decoder inputs were calculated as follows.

Counter Output	Weight
Q12	2048
Q11	1024
Q10	512
Q 5	16
Total	3600

The output of the decoder U2A sets the minutes R-S flip-flop (U1B and U1D) which applies a reset pulse through NOR gate U3B to counter U16. The next negative transition of the 60 Hz input resets the minutes R-S flip-flop, and the counter is free to count out another minute. Since state 3600 exists only momentarily, the counter effectively traverses states 0 through 3599.

The output of the minutes R-S flip-flop is used to clock the hour timer U17 and the four minute timer U20. Hour timer U17 consists of a CD4024A 7-stage binary counter and its associated hour decoder (U2B) and hour R-S flip-flop U4A and U3A. The required decoder inputs for a count of 60 were determined as follows:

3.4.2.2 (Continued)

Counter Output	Weight
Q6	32
Q5	16
Q4	8
Q3	4
Total	60

The output of the hour R-S flip-flop is routed through an inverter from U3A instead of directly from U4A because the set pulse from the hour decoder is only a transient, and it can be widened and made more reliable by running the signal through two extra gate propagation delays. State 60 is only momentary, and the counter effectively traverses states 0 through 59. The hour R-S flip-flop is reset on the next negative transition of the inverted clock pulse. The resultant hourly pulse from the hour R-S flip-flop is used to set the status flip-flop.

Now that the basic timing pulses have been described, the action resulting from a transition of the conditioned sensor indication will be described. If a positive transition occurs, the alarm D flip-flop will be cleared, causing a high logic level on the D input, pin 5 of flip-flop U7. On the next positive transition of the 60 Hz input, flip-flop U7 will be set, causing a high level from the Q output (pin 1) to be applied to the preset input (pin 6) of alarm flip-flop U6, causing it to be set. A low logic level will then be applied to the D input (pin 5) of U7, and on the next positive transition of the 60 Hz input, flip-flop U7 will be cleared, and the alarm D flip-flop will be stable until the next positive transition of the conditioned sensor indication. A pulse which is one clock period wide has been generated at U7 pin 2. This pulse (1) sets the alarm R-S flip-flop (U8D and U22B), (2) resets the minute timer U16 so that its first output will occur in one full minute, (3) resets the secure R-S flip-flop (if not already reset), (4) presets four minute timer U20 through NOR gate U8C, (5) removes the clear input from enable counter U19 by setting the enable flip-flop (U21C and D) through NOR gate U22A, and (6) enables the parallel loading of the output shift register, U24, 33, 36, 38, and 40. The parallel inputs of the output shift register are dervied from user ID code plugs 1 and 2 which pull down selected inputs, from the secure R-S flip-flop which iuputs a low level for alarm and a high level for secure, and from the status flip-flop which inputs a high level for a routine hourly report and a low level otherwise.

3.4.2.2 (Continued)

At the end of the pulse from U7 pin 2, (1) the output shift register switches to the serial mode, shifting out data to the transmitter from U24 pin 3 through multiplexer U9A, B, and C, (2) the enable counter U19 starts counting and (3) parity flip-flop U23A, starting from a reset state, switches state everytime a high-level bit appears at U24 pin 3, the output of the output shift register. After all 40 bits originally parallel loaded into the output shift register have been shifted out, decoder U5A places a low level on the D input of mux flip-flop U23B, causing it to reset on the next 60 Hz input and select the serial output from the parity flip-flop U23A instead of the output shift register, thus appending a parity bit at the end of the word. Two clock pulses later, the enable flip-flop is reset by decoder U5B, ending the enable gate to the transmitter, resetting the parity flip-flop, and presetting the mux flip-flop to make the multiplexer select the output shift register as the serial output. All this takes about two-thirds of a second.

After the pulse from U7 pin 2 ends, four-minute timer U20 starts counting the minute pulses arriving at its clock input by way of NAND gate U4C. U20 is preset to state 4 and counts down. While the four-minute timer is counting down, every minute pulse is gated through NAND gate U21B and NOR gate U22A to parallel load the output shift register and set the enable flip-flop just as the original pulse from flip-flop U7A did. Four-minute timer U20 is clocked on the trailing edge of the minute pulse, so the output shift register is loaded and the four minute timer decrements to 3, loads and decrements to 2, loads and decrements to 1, loads and decrements to 0. When the 0 state is reached, the carry out output of U20 goes low, gating off further minute pulses through gates U21B and U4C, resetting (if set) the alarm R-S flip-flop and the secure R-S flip-flop, and enabling a status transmission when the hour timer times out.

If the conditioned sensor indication produces a negative transition, the secure D flip-flop is cleared, and the whole procedure of loading, enabling, shifting, and parity generation for five transmissions occurs just as with a positive sensor transition except that the alarm R-S flip-flop is reset and the secure R-S flip-flop is set. Since the alarm/secure bit is derived from the secure R-S flip-flop, that bit will be high instead of low as in an alarm.

3.4.3 Sensor Transmitter Mechanical Design

The sensor transmitter (S/T) housing was made larger than originally proposed because of the space required for the discrete components and the mounting of the tamper switch. A mechanical drawing of the S/T is shown in Figure 3-24. The objective was the ability to plug the S/T into an existing ac outlet without losing the use of the outlet. This was accomplished by providing two ac outlets at the top of the housing which could be used to plug in appliances while the S/T was an active part of the BAS. Because tooling for low quantity plastic housings was prohibitive, a metal can was used. Using metal created a potential safety problem because of the ac voltage being conducted within the housing. Therefore, adequate clearance had to be provided to prevent accidental shocks. This too, contributed to the overall size of the breadboard model. In production, the housings would definitely have to be fabricated from a plastic material.

Although the ultimate size of the S/T can easily be reduced by virtue of micro-miniaturization, the problem of detecting a tamper alarm by turning the locking screw still remains.

Double outlets are not as universal as one might think. There are two types in general use for residential households: the older dual receptacle without the ground terminal and the newer ones with the center grounding terminal. The problem arises in the fact that the distance from the center of the blade receptacle to the center screw hole is different for each receptacle.

Because of the manner which the S/T plugs into the wall outlet, the location of the hold-down/tamper detector screw is fixed. It can be located to accept the old or new dual outlet; but not both. For this reason a universal, plug-in S/T that uses the locking screw as a tamper mechanism is a real design challenge.

3.5 EXTERNAL INTERFACE

3.5.1 Functional Description

The external interface is used to interface serial data from the communication interface at the central processor with a 600 Ω telephone line. This is done in order to provide the user with an optional coupling to a central monitoring station. A block diagram/schematic of the unit is shown in Figure 3-25 while a photograph of the equipment is shown in Figure 3-26.

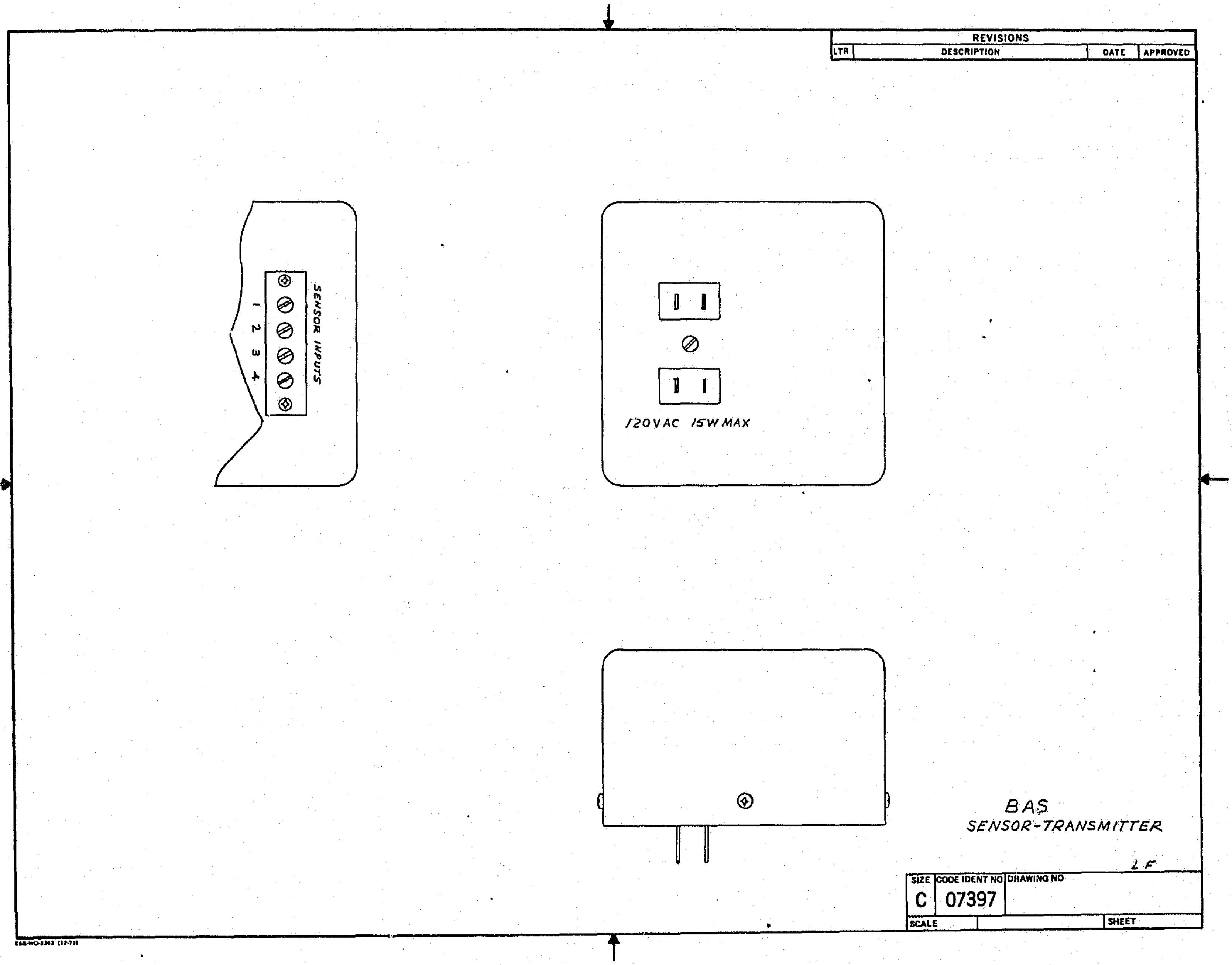

Figure 3-24. Sensor Transmitter Assembly

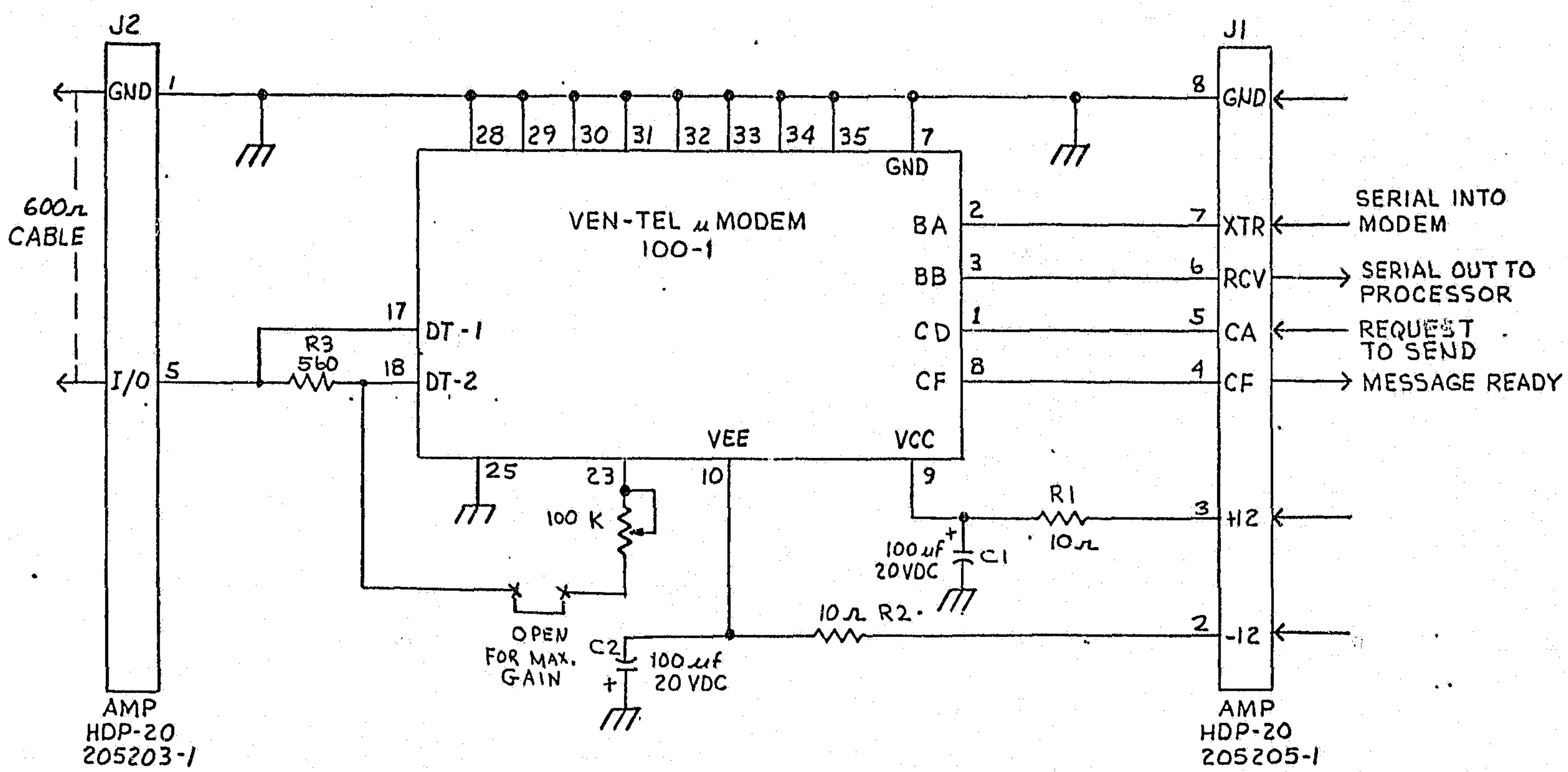

Figure 3-25. External Interface Block Diagram/Schematic

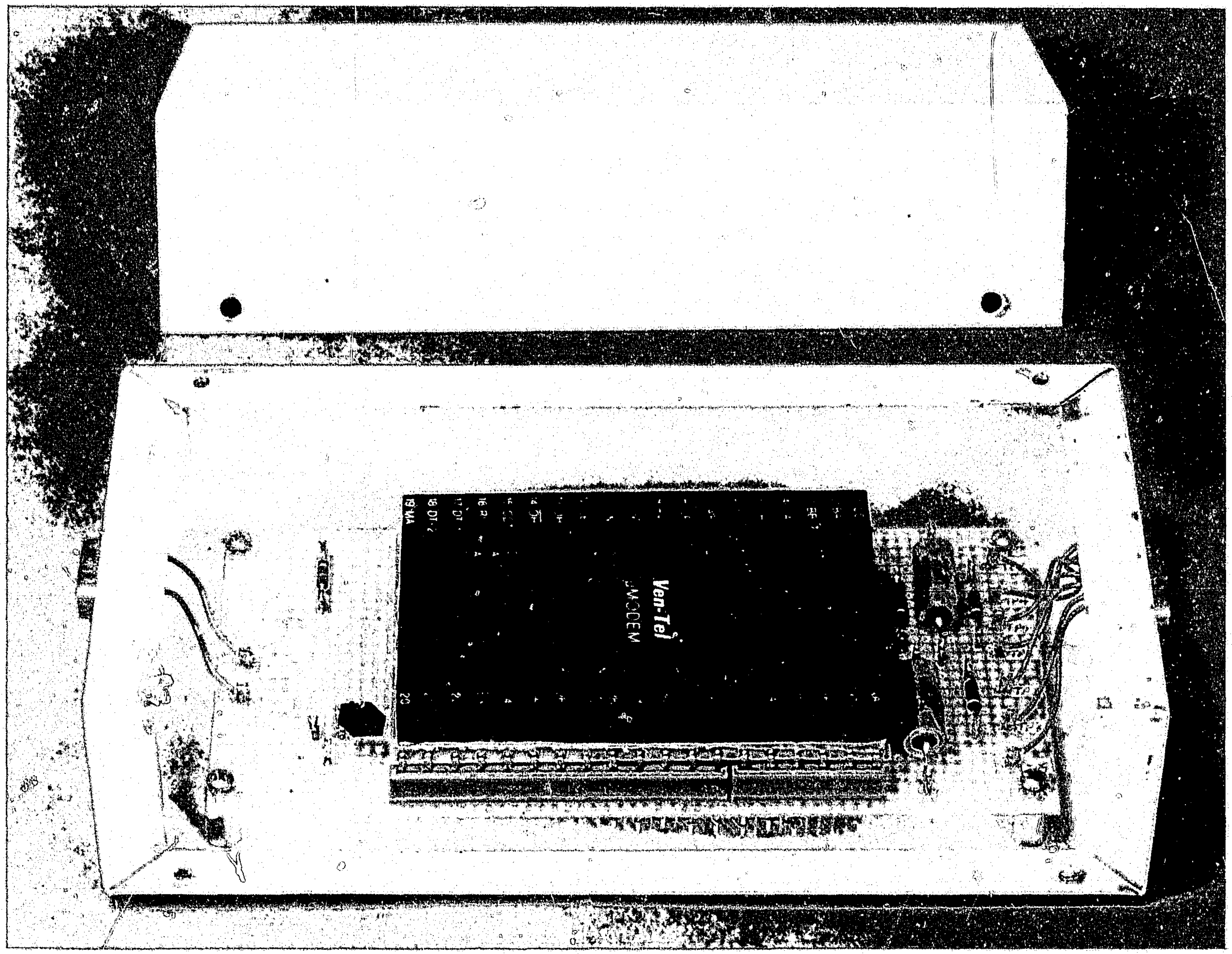

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Figure 3-26. External Interface

3.5.2 External Interface

The external interface housing was simply an off-the-shelf wrap-around case as shown in Figure 3-27. It was used to house the modem and a few electronic components. The modem was mounted on a perforated board and held in place by four standoffs. A different size, keyed connector was assembled, one on each end of the metal housing.

In production, the modem and its associated circuitry would be packaged within the processor and would be offered as an option.

3.6 CENTRAL STATION

3.6.1 Functional Description

The central station is used to simulate a remote monitoring station such as a central monitoring alarm station. Its purpose is to demonstrate both the ability to interrogate each of the burglar alarm systems and to receive alarms when generated by the burglar alarm systems. It communicates with the BAS's through modems connected to a 600 Ω transmission line which simulates a telephone hookup.

The central station block diagram is shown in Figure 3-28 and photographs of the unit are shown in Figures 3-29 and 3-30.

3.6.2 Circuit Descriptions

The central station is comprised of a microprocessor, an I/O matrix, a communication interface, a front panel and a power supply. These circuits are described in the following subsections and reference schematic diagram SK00-3423 in Appendix A.

3.6.2.1 Microprocessor

The microprocessor in the central station is identical to the one used in the central processor with the exception that U6, and U9 are not installed due to a smaller program requirement. This microprocessor was previously discussed in Section 3.2.2.1 and a schematic diagram is given as SK00-3415 in Appendix A.

3.6.2.2 I/O Matrix

The I/O matrix at the central station (schematic SK00-3423 in Appendix A) is similar to that used in the central processor. The user ID for both BAS systems are provided as inputs to the central station. Four front panel switch positions

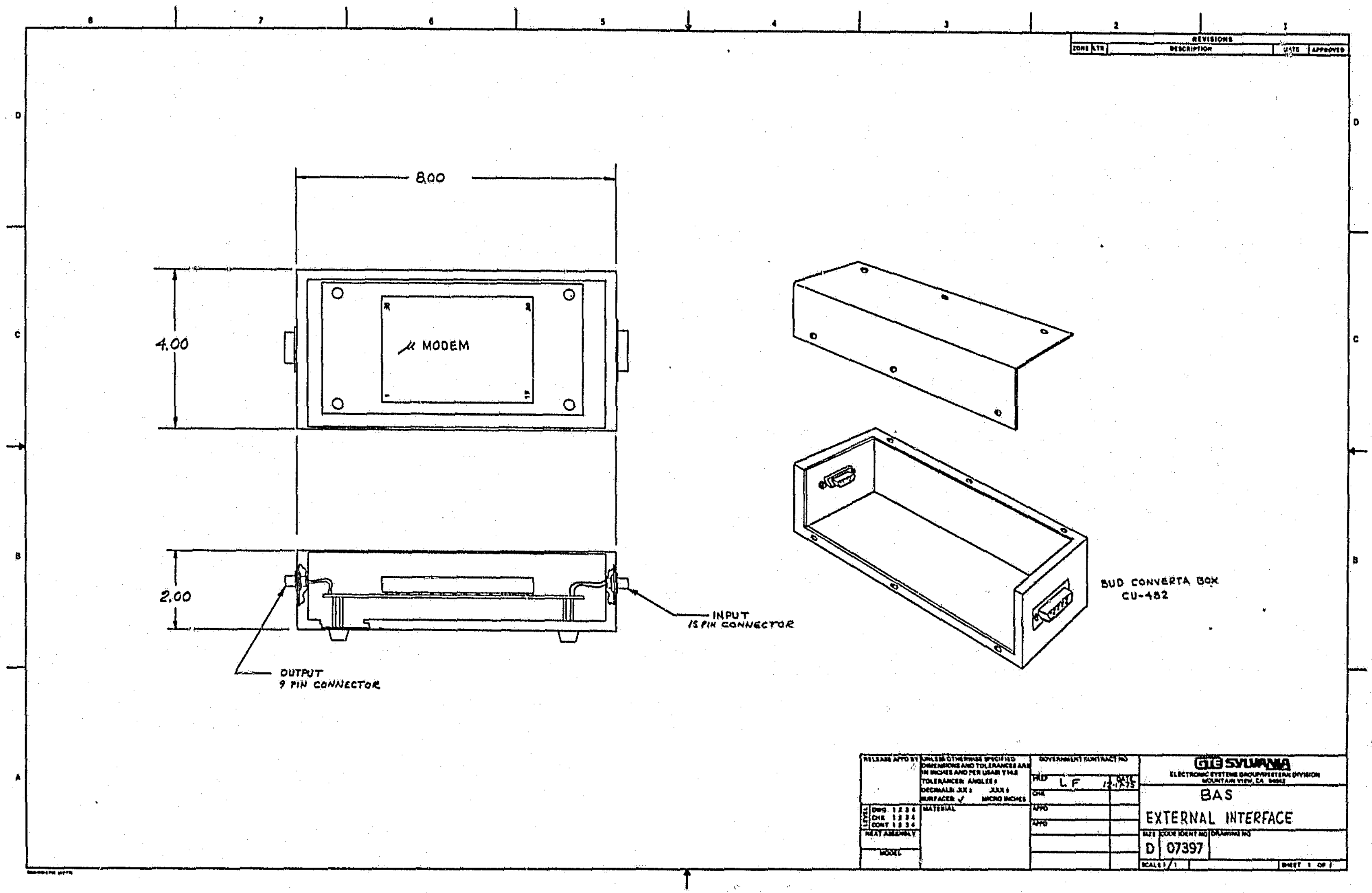

Figure 3-27. External Interface Assembly

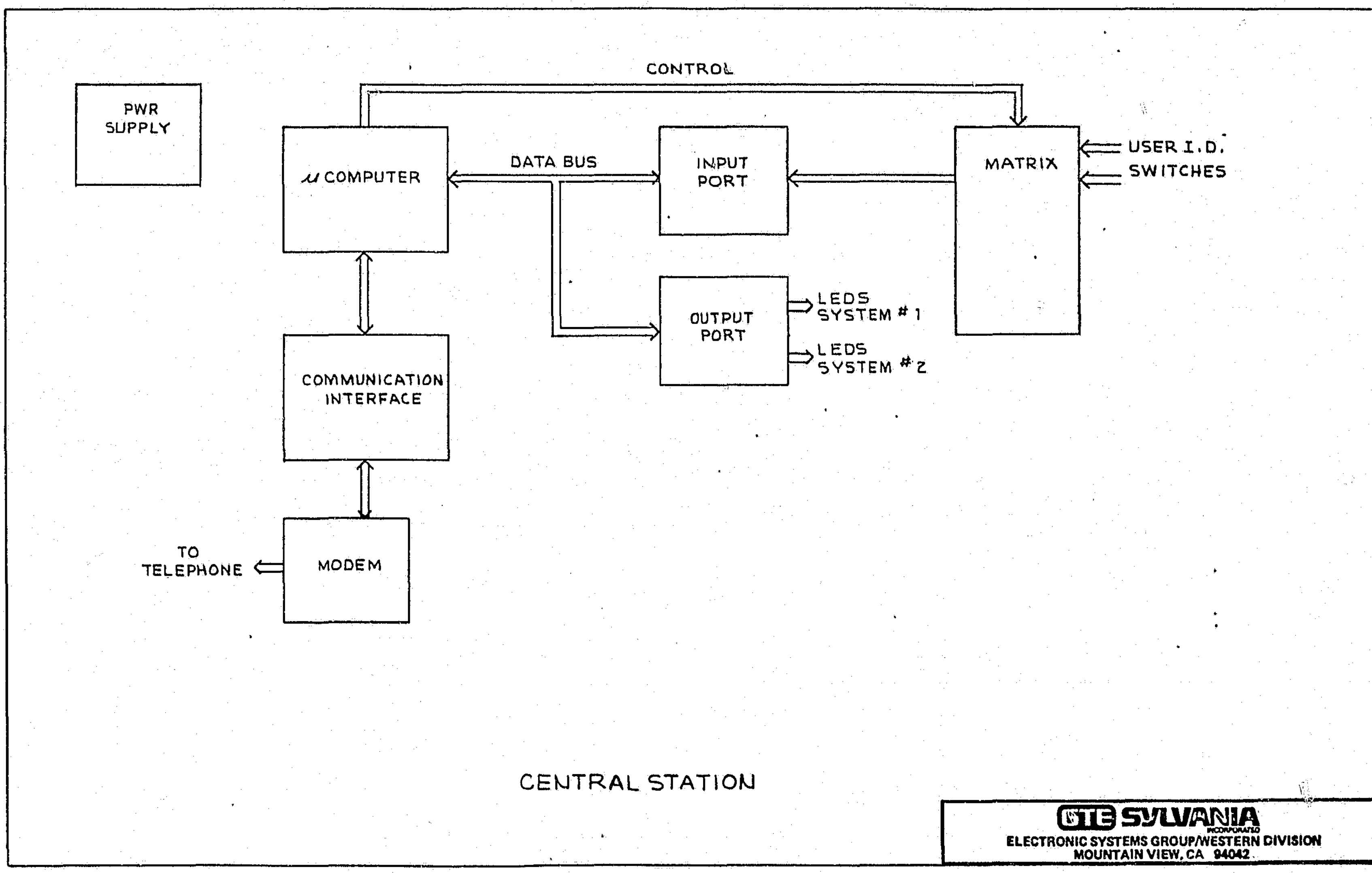

Figure 3-28. Central Station Block Diagram

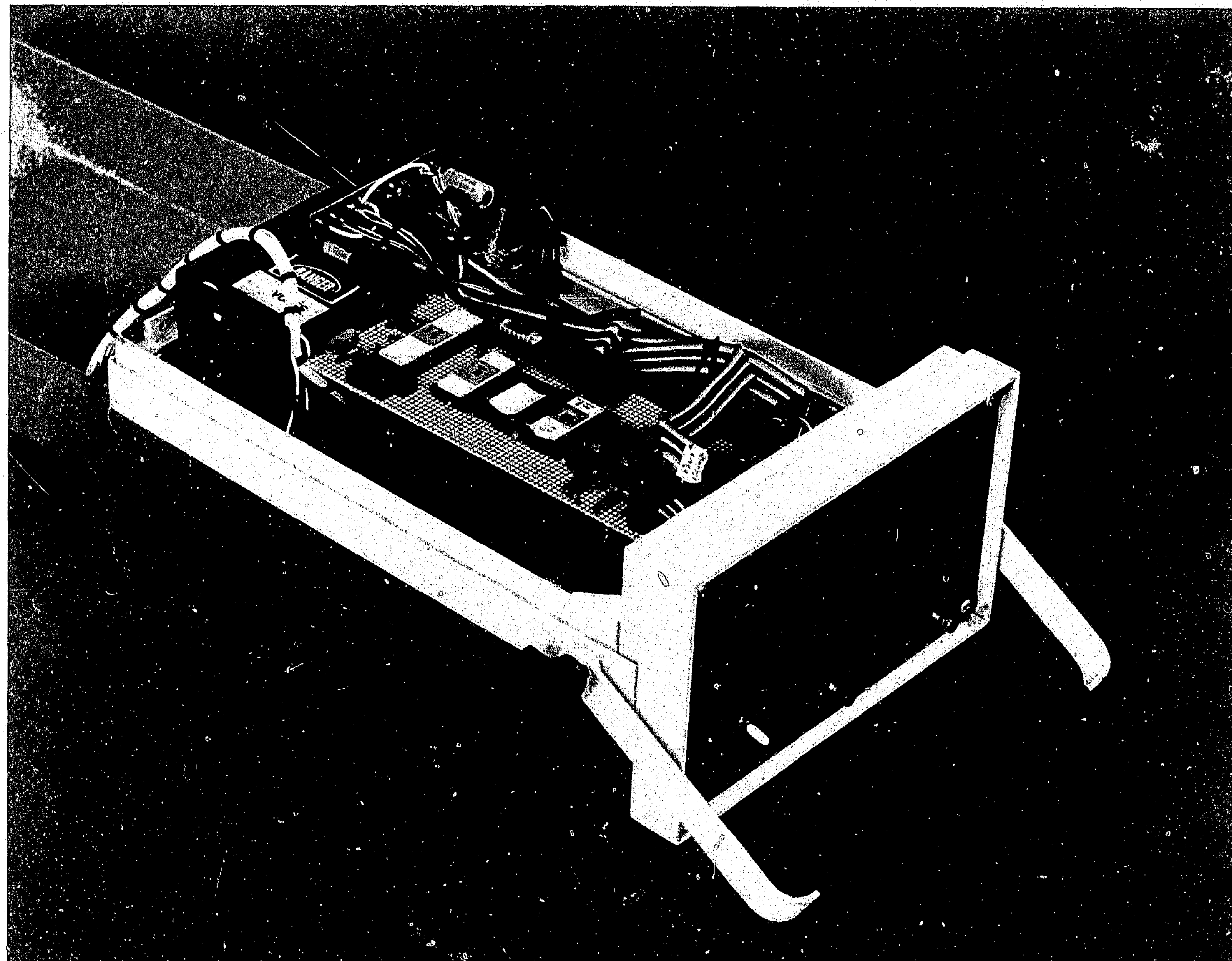

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Figure 3-29. Overall View of Central Station with Top Removed

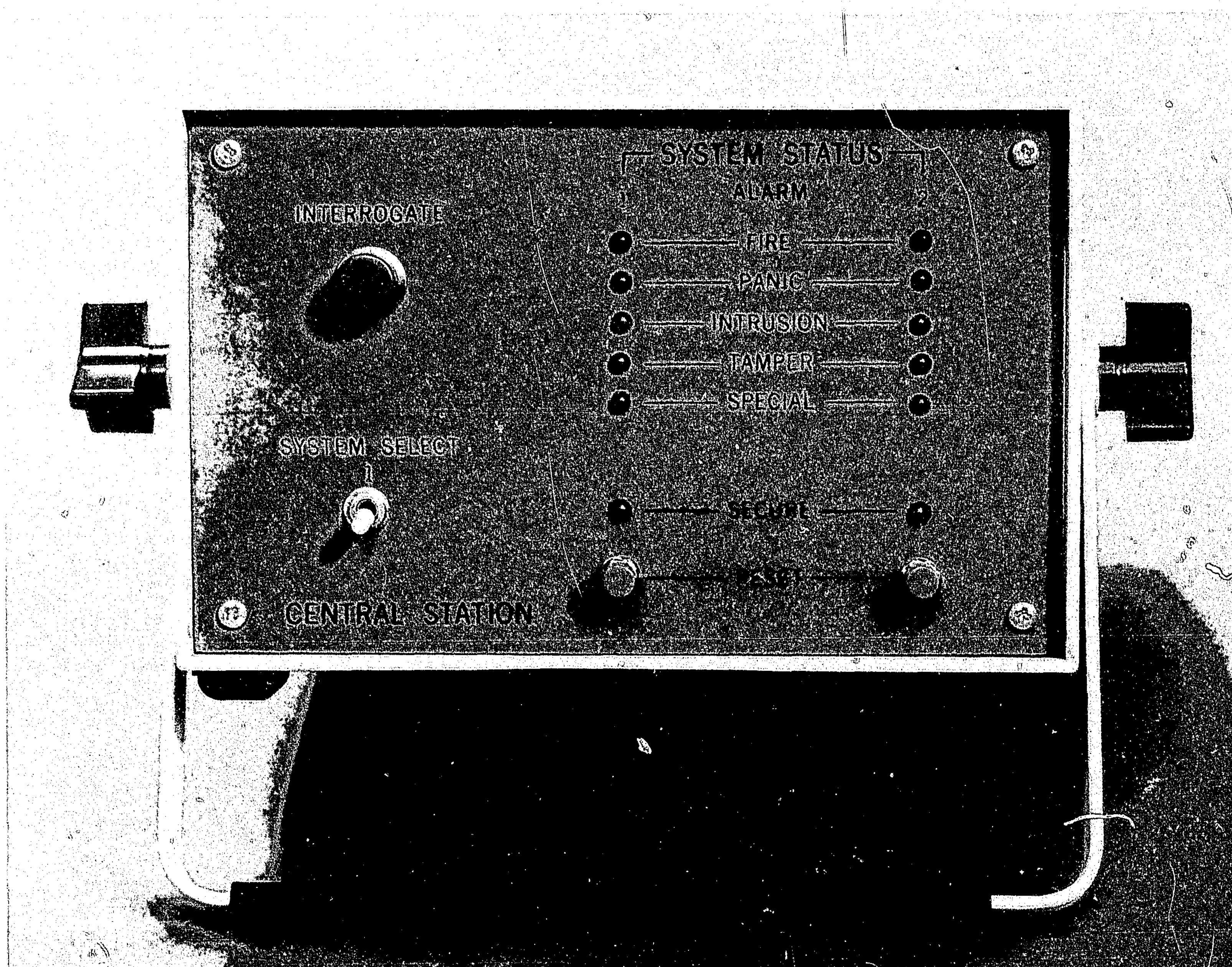

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Figure 3-30. Central Station Front Panel

3.6.2.2 (Continued)

also provide inputs to the system. The "system select" switch tells the processor which system to interrogate when the interrogate button is depressed. The "Reset 1" and "Reset 2" pushbutton switches resets the alarm indication lights on the front panel. The two output ports U2 and U3 drive the LEDs on the front panel to indicate system status.

3.6.2.3 Communication Interface

The only communications interface required at the central station is that required to interface with a telephone line via the Ven-Tel micro modem model 100-1. This interface is identical to that used in the central processor previously described in Section 3.2.2.4. The major exception is that the central processor communications interface required a link to the powerline communications as well. This circuitry is not applicable to the central station. In addition, the Ven-Tel modem is physically located within the central station housing instead of being housed in an external interface as is done with the central processor.

3.6.2.4 Front Panel

The front panel (schematic SK00-3423) of the central station is shown in Figure 3-30. When an alarm occurs in either of the burglar alarm systems the appropriate light for that type of alarm for that system will light up. There is no audio indication of an alarm condition at the central station. These lights may be reset by depressing the appropriate reset button at the bottom of the column of lights. The central station also automatically interrogates each of the burglar alarm systems on an hourly basis and one of the lights will light up, depending on the status of the BAS's. If there is no alarm condition the secure light will be illuminated. If system status is desired at any other time the systems may be interrogated by selecting the desired system with the system select switch and depressing the interrogate button. The system select switch is only used for this purpose.

3.6.2.5 Power Supply

The central station power supply is identical to the central processor and entrance control power supplies with the exception that it does not incorporate a bell drive or a strike release power supply.

3.6.3 Central Station Mechanical Design

The housing for the central station was simply chosen to provide a sturdy envelope for the central station breadboard. A production central station would probably be minicomputer based and provide hard copy alarm readouts. The size, although not overly large, was picked because of the volume required for the breadboard electronic components. The central station was made into a two-channel annunciator because only two systems were delivered, however; a production version would probably be multichannel and fully automatic. The housing used was a vendor-supplied case which was lightweight and easily disassembled. An assembly drawing of the central station is shown in Figure 3-31.

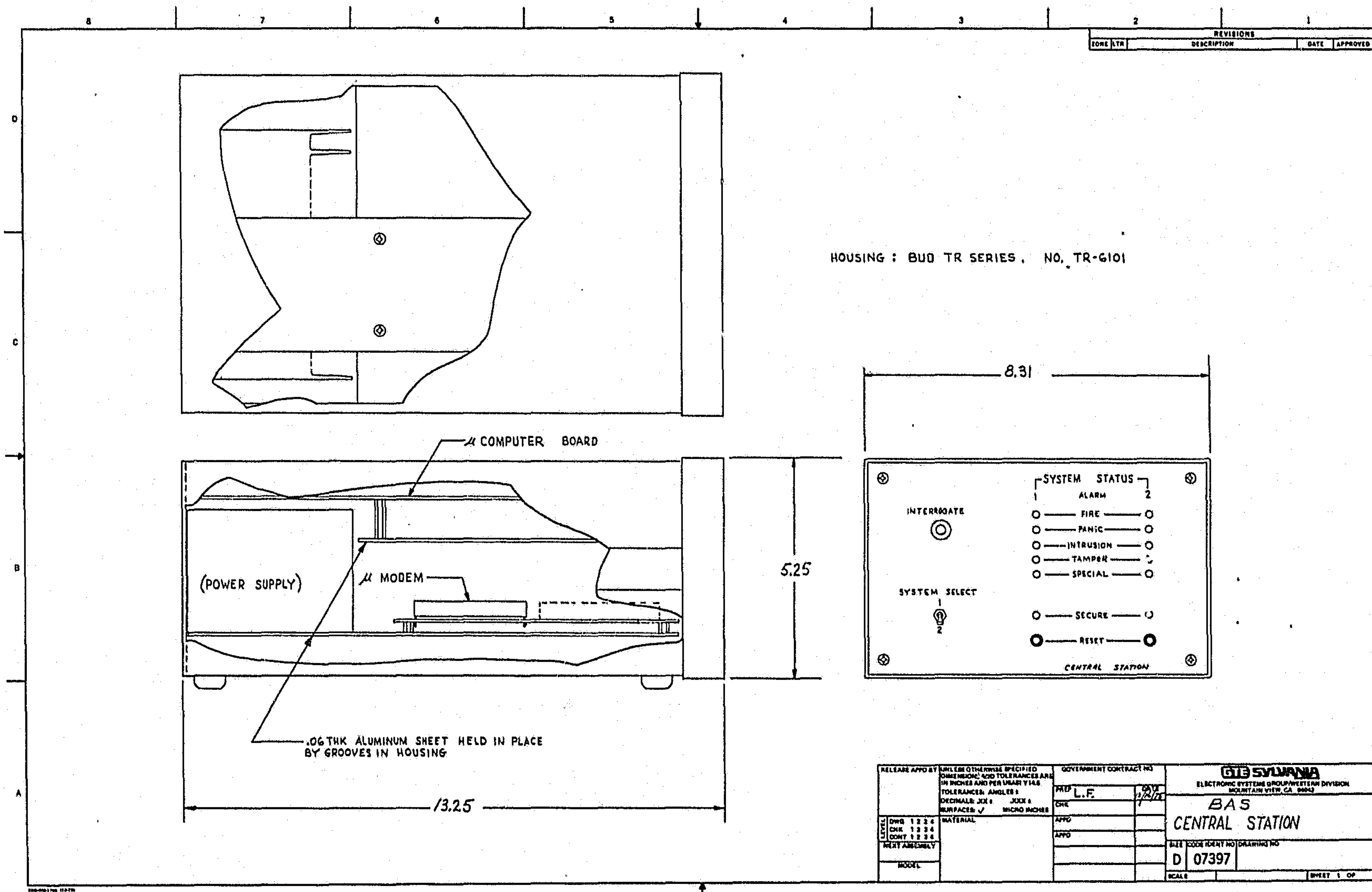


Figure 3-31. Central Station Assembly

CHAPTER IV. SOFTWARE DEVELOPMENT

4.1 GENERAL

The philosophy behind the software design and development was to substitute software for hardware wherever possible. The timing logic originally set forth in the system concept phase, allowed for slower speeds of data handling and control. Software implementations in place of hardware involved a compromise on speed, while in most cases such tradeoffs provided a simpler and less expensive system (i.e., reduced hardware chip count). Thus, except for the simplest of hardware I/O (input and output) all timing, control, and system logic was done in software, using the INTEL 8080 microprocessor.

4.1.1. Microprocessor

The first consideration in the design of the BAS system was the choice of a microprocessor to implement the software portions of the system. The primary concern was to select a low power microprocessor. However, during the initial design of the BAS system, the low power microprocessor had not yet established itself on the microprocessor market, even though there were several companies anticipating the marketing of their own low power microprocessor in the near future. Since the initial systems were to be feasibility models, power was considered to be expendable for the first breadboard systems. Consequently, the INTEL 8080 was selected as the system microprocessor because of the extensive amounts of hardware and software support available and because of previous in-house 8080 experience and support.

4.1.2 Techniques

In general, much of the software used stacking and polling techniques. Stacks and queues were employed in storing active sensors, trouble indicator (TI) error codes, handshaking between the central processor and entrance control, entrance control combination transmission and central station interrogation. Polling was determined to be the best I/O technique over interrupt and DMA (Direct Memory Access), first, for the unnecessary additional speed that the other techniques presented

4.1.2 (Continued)

and second, for the additional hardware involved in interrupt and DMA handling. I/O polling was used in the external interfacing with the powerline and modem, switch reading, and control flip-flops.

4.1.3 Input/Output

I/O handling was done both in parallel and in series. All switches and control flip-flops used eight bit I/O ports to input and output bits in parallel. Tables 4-1, 4-2, and 4-3 give a list of the I/O ports and their corresponding bits. Power line and modem data used a bidirectional eight bit shift register for serial input and output. Bit 0 was used for serial input and bit 7 was used for serial output. Because the hardware did not allow for simultaneous I/O in the central processor or entrance control, a priority was established for power line and modem I/O. Power line transmissions received the highest priority because of the need for quick response in system handshaking. The modem receiver was determined to have the next highest priority, unless an interrogate message had been previously received, then the modem receiver was ignored until the loss of the carrier. Modem transmissions were selected to have the third highest priority because of the low probability that long periods of time (10 seconds) would occur which would not have short non-active periods of the power line transmitter or modem receiver activity; these non-active periods could be used for modem transmission. Lowest on the list of priorities was the power line receiver. If a power line message was missed because one of the higher priority I/O activities, it would eventually be received because of the multiple message structure of all transmitting, that is, all sensor and handshaking messages have multiple transmissions at timed intervals.

4.1.4 Handshaking Dialogue

The purpose of handshaking is to set up a common eight bit codeword in the central processor and entrance control so that combination digits from the entrance control could be encoded using the codeword when transmitting to the central processor. Each digit, which is a four bit binary word from 0-11, is encoded using modulo 2 addition (exclusive OR) between the digits and the upper and lower four bits of the codeword alternately (see Table 4-4). Each new codeword, which is essentially an

Table 4-1. Central Processor Eight-Bit I/O Ports

Input Port 1	=	Power line and modem receiver data		
		Bit 0	=	New data bit shifted in
Input Port 2	=	Keyboard		
		Bits 0-7	=	Keys 1, 4, 3, *, 2, 5, 8, 0, respectively
Input Port 3	=	Keyboard, tamper switch, and I/O condition flags		
		Bits 0-3	=	Keys 3, 6, 9, #, respectively
		Bit 4	=	Bell and processor tamper
		Bit 5	=	Carrier
		Bit 6	=	Clock
		Bit 7	=	Phase lock
Input Port 4	=	ID #		
Input Port 5	=	ID #		
Input Port 6	=	Entrance control, special, and parameter sensor code plugs		
		Bit 0	=	Entrance control #1
		Bit 1	=	Entrance control #2
		Bit 2	=	Special #1
		Bit 3	=	Special #2
		Bit 4	=	External #1
		Bit 5	=	External #2
		Bit 6	=	External #3
		Bit 7	=	External #4
Input Port 7	=	Mode switches, illuminate/arm button, and run/start switch		
		Bit 0	=	All mode
		Bit 1	=	Door/windows mode
		Bit 2	=	Run/start switch
		Bit 3	=	Remote mode
		Bit 4	=	Local/remote mode
		Bit 5	=	Local alarm mode
		Bit 6	=	Local alert mode
		Bit 7	=	Illuminate/arm button
Input Port 8	=	Combination		
		Bits 0-3	=	4th digit
		Bits 4-7	=	3rd digit
Input Port 9	=	Combination		
		Bits 0-3	=	2nd digit
		Bits 4-7	=	1st digit
Output Port 1	=	Power line and modem transmit		
		Bit 7	=	Data to be shifted to transmitter
Output Port 2	=	Mode LEDs		
		Sensor Modes:		
		Bit 0	=	All
		Bit 1	=	Doors/windows
		Bit 2	=	Fire/panic
		Alarm Modes:		
		Bit 3	=	Remote
		Bit 4	=	Local/remote
		Bit 5	=	Local alarm
		Bit 6	=	Local alert
		Bit 7	=	Test
Output Port 3	=	I/O control, arm and access lights, local alert and bell		
		Bit 0	=	Z4 I/O control
		Bit 1	=	Z5
		Bit 2	=	Bell alarm on
		Bit 3	=	Pulsing or steady alert
		Bit 4	=	Alert on
		Bit 5	=	Access light
		Bit 6	=	Armed light
		Bit 7	=	Receiver and transmitter clock control
Output Port 4	=	Trouble indicator LED		
		Bits 0-3	=	Low BCD digit
		Bits 4-7	=	High BCD digit

Table 4-2. Entrance Control Eight-Bit I/O Ports

Input Port 1	=	Power line and modem receiver data		
		Bit 0	=	New data bit shifted in
Input Port 2	=	Keyboard		
		Bits 0-7	=	Keys 1, 4, 7, *, 2, 5, 8, 0, respectively
Input Port 3	=	Keyboard, tamper switch, and I/O condition flags		
		Bits 0-3	=	Keys 3, 6, 9, #, respectively
		Bit 4	=	Bell and processor tamper
		Bit 5	=	Carrier
		Bit 6	=	Clock
		Bit 7	=	Phase lock
Input Port 4	=	ID #		
Input Port 5	=	ID #		
Input Port 6	=	Entrance control #1 or 2		
Input Port 7	=	Switches		
		Bit 0	=	Arm
		Bit 1	=	Panic
		Bit 2	=	Door
Output Port 1	=	Power line and modem transmit		
		Bit 7	=	Data to be shifted to transmitter
Output Port 3	=	I/O control, strike release, and TI light		
		Bit 0	=	I/O control
		Bit 1	=	Strike release
		Bit 2	=	TI light
		Bit 7	=	Clock control

Table 4-3. Central Station Eight-Bit I/O Ports

Input Port 1	=	Power line and modem receiver data		
		Bit 0	=	New data bit shifted in
Input Port 2	=	System 1 = ID #2		
Input Port 3	=	I/O control number and switches		
		Bit 0	=	Reset system 1
		Bit 1	=	Reset system 2
		Bit 3	=	System select bit 2 = interrogate
		Bit 5	=	Carrier
		Bit 6	=	Clock
Input Port 4	=	System 1 = ID 32		
Input Port 5	=	System 1 = ID #1		
Input Port 6	=	System 2 = ID #1		
Output Port 1	=	Power line and modem transmit		
		Bit 7	=	Data to be shifted to transmitter
Output Port 2	=	System 1 lights		
		Bit 2	=	Fire light
		Bit 3	=	Panic light
		Bit 4	=	Intrusion light
		Bit 5	=	Tamper light
		Bit 6	=	Special light
		Bit 7	=	Secure light
Output Port 3	=	System 2 lights and I/O control		
		Bit 1	=	Transmitter control
		Bit 2	=	Fire light
		Bit 3	=	Panic light
		Bit 4	=	Intrusion light
		Bit 5	=	Tamper light
		Bit 6	=	Special light
		Bit 7	=	Secure light

Table 4-4. Modulo 2 Addition for 4-Digit Combination, 1976

Example: Combination = 1-9-7-6				Codeword = 01100011			
Entrance Control Digit Encoding				**Central Processor Digit Decoding**			
1st Digit:							
(DIGIT #1)	$\oplus$	(1st half of codeword)	= Encoded digit	(Encoded digit)	$\oplus$	(1st half of codeword)	= Digit 1
0001	$\oplus$	0110	= 0111	0111	$\oplus$	0110	= 0001
2nd Digit:							
(DIGIT #2)	$\oplus$	(2nd half of codeword)	= Encoded digit	(Encoded digit)	$\oplus$	(2nd half of codeword)	= Digit 2
1001	$\oplus$	0011	= 1010	1010	$\oplus$	0011	= 1001
3rd Digit:							
(DIGIT #3)	$\oplus$	(1st half of codeword)	= Encoded digit	(Encoded digit)	$\oplus$	(1st half of codeword)	= Digit 3
0111	$\oplus$	0110	= 0001	0001	$\oplus$	0110	= 0111
4th Digit:							
(DIGIT #4)	$\oplus$	(2nd half of codeword)	= Encoded digit	(Encoded digit)	$\oplus$	(2nd half of codeword)	= Digit 4
0110	$\oplus$	0011	= 0101	0101	$\oplus$	0011	= 0110

4.1.4 (Continued)

eight-bit binary number is generated randomly to prevent an intruder from easily decoding the combination. Thus, a new codeword is established by the handshake procedure each time the system is armed or powered up.

Handshake messages differ from sensor messages in that the ID data field contains data (codeword, encoded digit, or trouble indication) instead of a sensor number. The subtype field is used to indicate which handshake message is being received. When the handshake procedure is initialized from the entrance control by pressing the arm button and closing the door, an arm request is sent to the central processor to start the generation of a new codeword. When the central processor receives an arm request, or if the system is powering up, the central processor will begin the handshake process and handshake with each entrance control in the system. The handshake process for each entrance control is started first by the selection of a random codeword by the central processor. The first four bits of the codeword are then transmitted to the entrance control in a DATA 1 handshake message. Upon receiving a DATA 1 message, the entrance control temporarily stores the four codeword digits and sends the four digits back to the central processor via a CONFIRM 1 message. If the central processor does not receive a CONFIRM 1 message within two seconds or the four digits received in the CONFIRM 1 message are not the same as in the DATA 1 message, then the central processor repeats the DATA 1 message for a minimum of four times or until a correct CONFIRM 1 is received. If a correct CONFIRM 1 is not received on the fourth try then the handshaking for the entrance control is aborted, an error code is set in the trouble indication stack, and the old codeword is assumed to be the new one.

When a correct CONFIRM 1 is received by the central processor then the program will transmit the second half of the codeword to the entrance control in a DATA 2 message. The same sequence occurs in the DATA 2 message as with DATA 1 message except when the entrance control receives a DATA 2 the entrance control replaces the old codeword with the new codeword from the DATA 2 and last DATA 1 message. Handshake aborting also occurs if the central processor fails to receive a correct CONFIRM 2 message after four attempts. Finally, when a correct CONFIRM 2 is received by the central processor, the old codeword is replaced by the new one and an OK message is sent to the entrance control. The OK message also contains a

4.1.4 (Continued)

trouble bit to indicate if there is trouble within the system (i.e., user error, masked sensor, alarm, etc.). The entrance control will turn on the trouble indication light for twenty seconds after receiving an OK message. If the trouble indication bit is set, then the light will flash to indicate trouble in the system; otherwise, the light will be steady. (See Figure 4-1.) After the central processor sends an OK message, handshaking will begin with the next entrance control.

To enter and disarm from an entrance control the user must enter the four correct digits (predetermined by the codeplug in the central processor) at the entrance control keyboard and wait for the strike release. The entrance control will take the digits from the keyboard, encode them, and transmit each one to the central processor. When the central processor receives and decodes the fourth digit, the system will be disarmed and a STRIKE RELEASE message will be transmitted to the entrance control. The trouble indication bit is handled in the same manner as in the OK message; however, the entrance control will also turn on the strike release for five seconds when it receives a STRIKE RELEASE message.

Flow diagrams for all software is given in Appendix B while a program listing is given in Appendix C.

The next sections will discuss the specific software routines generated for the central processor, the entrance control and the central station respectively.

4.2 CENTRAL PROCESSOR

4.2.1 Power Up

During power up RAM (random access memory) is initialized, that is, all flags, buffers, stacks, and variables are set to an initial state that assumes the system has no alarm or status errors. A flag is set and an error code set in the trouble indicator stack to indicate that power has just been restored. Next, the run switch is read. If the run switch is in the run position then the microprogram will begin the arming sequence which includes entrance control handshaking; otherwise, the program will wait for the run switch to be switched from the start position to the run position. When the switch is moved from the start position, the processor will enter the access mode and after leaving the access mode the processor will also go through entrance control handshaking. Thus, after power up the central processor always establishes a dialogue between it and the entrance controls.

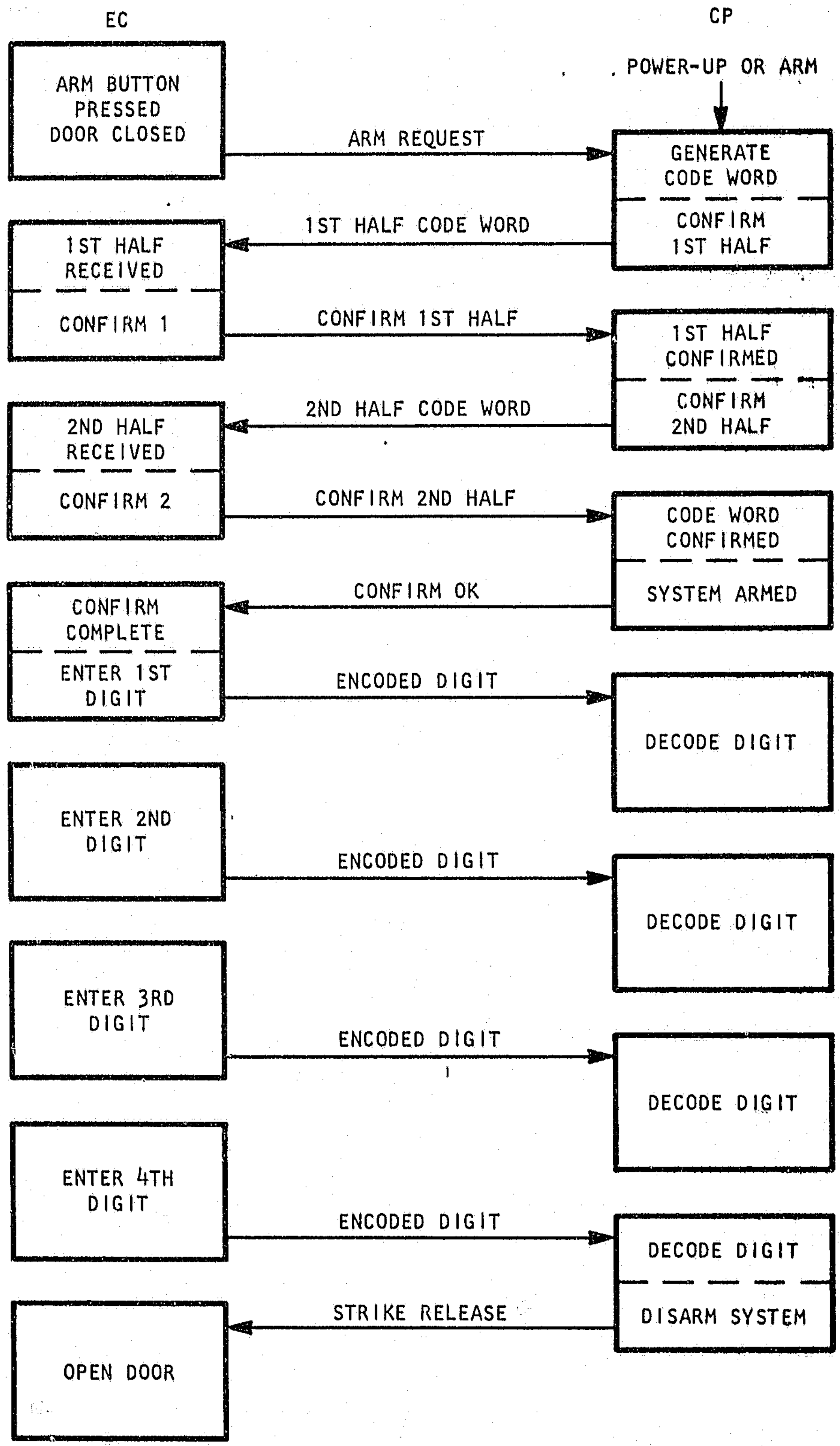


Figure 4-1. Central Processor and Entrance Control Handshaking

4.2.2 Access Mode

Upon entering the access mode (SACC) which is accomplished by inputing the four-digit user combination at the central processor keyboard, the central processor will first disable the processor and bell tampers, turn on the access light, and start a one minute access timer. The access mode will not terminate until the processor and bell tampers are secure. Consequently, the processor will only terminate the access mode after the expiration of the access timer or the pressing of the arm button, whichever comes first, and the securing of the tampers. Also, except when a processor (or bell) tamper is in progress, all alarms will be aborted after entering the access mode. This insures against an intruder forcing the processor door open, reading the combination, and entering the access mode to shut off the alarms. Upon leaving the access mode the code plugs will be read (READ CP) the access and mode lights will be turned off, and the tamper will be enabled. If the power up flag is set then entrance control handshaking will occur, or if the arm button was pressed during the access mode the system will execute the arming routine (SARL) otherwise, the program will enter an unarmed state.

4.2.3 Main Polling Loop

The main polling loop checks for keyboard data, receiver messages, the arm button depression, processor (or bell) tamper switch, end-of-access mode, mode switch output if tamper is disabled (access mode), and timer expirations. When any key is pressed on the processor keyboard, the program will enter the key combination check routine (KEY) the program will enter the key combination check routine and decide whether the sequence of key inputs matches the correct combination. Similarly, when a receiver message, arm button closure, processor tamper, or end-of-access mode occurs the microprogram will enter the receiver message decoding (RECDAT), arm button pressed (ARMBUT), tamper alarm (GART), or End-of-Access (ENDACC) routines respectively. If the processor tamper is disabled, i.e., the system is in the access mode, the program will read and display the mode settings via the small LED indication lights. Also, if the system is armed the processor will turn on the ARM light. Table 4-5 is a list of the timers and what happens when they expire.

Table 4-5. Timer Functions and Executions

Timer	Function	Execution on Expiration
Access	1 minute - access mode timer	Reset access timer flag (End access mode if tamper secure)
Code	2 seconds - checks for confirm message from entrance control	Go to entrance control error routine (ECERR) (Failure in entrance control handshake)
Display	20 seconds - display present modes of the central processor	Turn off mode LEDs
Fire	5 minutes - fire alarm timer that sounds pulsating alarm	Turn off bell and alert and reset fire alarm in progress
Bell	5 minutes - general bell alarm timer	Turn off bell and reset tamper, panic, and intrusion alarm in progress
Local Alert	5 seconds - local alert time with counter to indicate successive multiple 5 second alerts	
	Intrusion alert count = five 25 second intrusion warning	Go to intrusion alarm routine (GARI)
	Arming delay count = fifteen 1-1/4 minute alert before arming	Go to arming routine (SARN)
	Special alert count = sixty 5 minute special alert	Turn off alert and reset special alarm in progress
Min 5	5 minutes - for updating the state bits in the sensor status bytes. These bits are used to keep track of a sensor's activity every 5 minutes	Status bytes changed Bit 2 = Bit 1 Bit 1 = Bit 0
Hour	1 hour - for updating sensor status	Status errors for each sensor are set if no status message has been received in the last two hours
Jamming	3 minutes - detect steady jamming on receiver (reset when no receiver activity)	Go to internal intrusion alarm (ALINT)

NOTE: Each timer has a flag to indicate if the timer is on or off and a 16-bit word to indicate when (in seconds) it expires.

4.2.4 Arming

When the system is "armed" the armed light will be lit and the intrusion alarms will be enabled according to the mode settings. The system can be armed either from the central processor or the entrance control depending on the system configuration and mode settings. As in the case where the system does not have an entrance controll all arming is done at the central processor. In such a case, arming is immediate in the test or local alert modes and a 1-minute 20-second local alert warning is sounded before arming, which allows the user to leave the premises, in the local alarm, local/remote, and remote models. Furthermore, in order to arm from the processor the user must enter into the access mode and press the illuminate/arm button. If the system includes one or more entrance controls handshaking always occurs before arming. In addition, certain mode settings preclude arming from the central processor or entrance control. For instance, the system with an entrance control can be armed from the central processor only if it is either in the test or local alert modes. If the system is either in the fire/panic, test, or access modes, the system will not arm from an entrance control. Again, a one minute 10-second local alert arming warning is sounded when arming in the local alarm, local/remote, or remote modes to warn any other occupants of the house or building that the system is arming. Also note that except for arming in the test mode, sensors that have state errors (sensor left in the alarm state) or status errors are masked out (disabled) from the system.

4.2.5 Illuminate/Arm Button

The illuminate/arm button has two purposes: it is used to arm the system at the central processor, and it is used to display the present mode settings and trouble indicator error codes. When the button is pressed while in the access mode, the access timer will be terminated, and upon leaving the access mode the central processor will attempt to arm the system. If the button is pressed while not in the access mode, the mode LEDs will display the present alarm and sensor modes for 20 seconds. Also, an error code will be displayed on the trouble indicator LED and upon each successive depression of the button the processor will display each successive error code in the trouble indicator stack.

4.2.6 Alarms

There are five basic alarms generated by the system: fire, panic, intrusion, tamper, and special. An intrusion alarm may be either external or internal with "jamming" being handled as an internal intrusion alarm. The sensor and alarm mode

4.2.6 (Continued)

settings allow the user to select which sensors (perimeter or "all") cause what type of alarm (local alert, local alarm, external alarm, or both local and external). The sensor modes (fire/panic, doors/windows, and all) affect only the intrusion alarms, indicating which intrusion sensors are to be armed, while fire, panic, tamper, and special sensors are always monitored. The "fire/panic" mode disables all intrusion alarms, the "door/window" mode enables only the external intrusion alarms, and the "all" mode enables all intrusion alarms, both external and internal. The alarm modes (test, local alert, local alarm, local/remote, and remote) influence the type of alarm output. Table 4-6 lists the alarms that correspond to each alarm mode.

4.2.7 Receiver Messages (RECDAT)

When a message (see Figure 4-3) is received on the power line the TYPE and ID data fields are compared to a list of active sensors. If there is no match-up then a receiver error count is kept (RECEVR) to indicate that there are messages being received that are from sensors which are considered inactive (their code plugs are still in the processor). When a complete message has been received the program first checks for an entrance control handshake or combination message and if such a message occurs then the program enters the entrance control message routine (see Section 4.1.4). Otherwise, upon receiving a sensor message the program examines the subtype field and sensor status bytes to determine whether the message is to generate an alarm or not. If a non-alarm message occurs the status and state bytes are updated and the corresponding trouble indicator error codes are updated, otherwise, when an alarm message is received the appropriate alarm routine is executed.

4.2.8 Receiver and Transmitter Polling

The I/O polling routine (IOPOLL) reads and writes data serially on each pulse of a 60 Hz clock. The clock is polled throughout the program to keep track of the number of clock pulses and thus the number of seconds is incremented on every 64 clock pulses (64 is used to keep the central processor timing structure out of phase with the rest of the system). The I/O priority (discussed in Section 4.1.3) is implemented using the phase lock carrier, and mode settings. During power line transmitting (the highest priority), all processing pauses until the complete message is transmitted.

Table 4-6. BAS Alarm Outputs

	FIRE	PANIC	INTRUSION	TAMPER	SPECIAL
TEST	20 second test light and local alert	20 second test light and local alert	20 second test light and local alert	20 second test light and local alert	20 second test light and local alert
LOCAL ALERT	5 minute pulsating local alert and bell alarm	5 minute steady bell alarm	5 second local alert	5 minute steady bell alarm	5 minute local alert
LOCAL ALARM	5 minute pulsating local alert and bell alarm	5 minute steady bell alarm	5 minute steady bell alarm	5 minute steady bell alarm	5 minute local alert
LOCAL/ REMOTE	5 minute pulsating local alert and bell alarm with modem transmission	5 minute steady bell alarm with modem transmission	5 minute steady bell alarm with modem transmission	5 minute steady bell alarm with modem transmission	5 minute local alert with modem transmission
REMOTE	5 minute pulsating local alert and bell alarm with modem transmission	5 minute steady bell alarm with modem transmission	modem transmission only	5 minute steady bell alarm with modem transmission	5 minute local alert with modem transmission

4.2.8 (Continued)

The program only allows central station interrogations to be received if the carrier is on, the processor is not in the access mode, and the processor alarm mode switch is in either the local/remote or remote modes. Also, when the central station interrogate message is received, the program will immediately transmit a status message back to the central station on the modem. Unlike the synchronous modem transmission (status message after interrogate), the asynchronous modem transmissions (status message after an alarm) will wait until the carrier drops before transmitting (see Figure 4-2). If no other I/O activity (transmitter or modem receiving) is occurring and the phase lock is on, the program will receive power line data. A receiver flag is set when a power line message is received with correct parity and ID match, so that the TYPE and ID DATA field can be checked (see Section 4.2.7).

Modem Status Message from Central Processor to Central Station

Preamble (300 millisecond delay)	ID #2	Status Bits	ID #1	
				Parity

Bit 4 = Fire
Bit 3 = Panic
Bit 2 = Intrusion
Bit 1 = Tamper
Bit 0 = Special

Modem Message (Interrogation) from Central Station to Central Processor

Preamble (400 millisecond delay)	ID #2	ID #1	
			Parity

Figure 4-2. Modem Message Format for Alarm and Interrogation Messages

4.2.9 Read Code Plugs (READCP)

When a new list of sensors is generated by reading the code plug inputs, the old status byte of a sensor is restored into the new status if the sensor has been in the system previously. If a sensor of the new list was not in the old list then a new status byte, that assumes the sensor is secure and has good status, is stored. The sensors are stored with their corresponding status bytes in a stack (list) of active sensors with null bytes (FF Hex) separating each group of sensors. For entrance control

4.2.9 (Continued)

sensors the status byte is replaced by a codeword (see Section 4.1.4). Thus, the sensor list contains seven groups of sensors: entrance control, entrance control tamper, entrance control panic, special, perimeter (including entrance control doors), internal, and fire. Sensor and alarm modes are read in with fire/panic and test modes, respectively, being the detault modes on switch errors. The combination digits are read in with the * equal to 10 (1010 binary) and the # equal to 11 (1011 binary) and digits 0-9 equal to their BCD equivalent.

4.3 ENTRANCE CONTROL

4.3.1 Power-up

The entrance control reads its code plugs once during a power-up cycle. Therefore, it is necessary to disconnect power if code plugs are changed.

4.3.2 Main Loop

The entrance control looks for receiver messages, arm request, sensor changes, keyboard data, and timer expirations and executes the appropriate routines. If the arm button has been pressed and the door is then closed the program will transmit an arm request to the central processor and set up a timer to send four subsequent arm requests to the central processor at three second intervals. When a sensor (tamper, panic, or door) changes state (alarm to secure, secure to alarm) the program transmits the corresponding message to the central processor and sets up a timer to send four subsequent messages at one minute intervals.

If the door has changed from secure to alarm, the keyboard lockout flag will be set. Next, the program checks for a keyboard digit on the key stack, if there is a digit present then the key will be "popped" off the stack and transmitted to the central processor. During handshaking all entrance control sensor transmitting is inhibited. The following is a list of entrance control timers:

1.	Tamper:	Four one-minute timers for sending entrance control tamper alarms
2.	Power:	Four one-minute timers for sending entrance control panic alarms
3.	Door:	Four one-minute time rs for sending entrance control perimeter alarms

4.3.2 (Continued)

4. Arm Request: Four three-second timers for sending arm request to the central processor

5. TI light: Twenty second timer for steady or flashing TI light

6. Strike Release: Five second timer for duration of strike release

7. Five minute timer for resetting key count

8. One hour timer for door status messages.

4.4 CENTRAL STATION

The central station is the simplest of the programs and consists of an hour timer for hourly interrogation of both systems, switch monitoring for knowing when to interrogate a system, and resetting the status alarm lights, receiver routine (similar to the central processor and entrance control) message decoding routines for outputting the status bits of a status receiver message, and a transmitter routine that shifts data out to the modem. When the interrogate switch is pressed the program will read the code plugs and system select switch and stack the appropriate system number to be interrogated on a transmitter stack which allows for the interrogation of several systems at once in sequence. The transmitter routine "pops" a system number from the transmitter stack, loads the transmitter buffer with the corresponding ID, and shifts the data serially to the modem. The central station is capable of receiving and transmitting simultaneously; thus, it can receive from one system and transmit to another at the same time (see Figure 4-2). When a message is received on the modem, the status bits of the status message are outputted to the system status-alarm lights. If there are no alarms the receiver light is turned on.

CHAPTER V. CONCLUSIONS AND RECOMMENDATIONS

Through the development of the two feasibility models of the Burglar Alarm System, it has been shown that all previously established requirements can and have been met. This includes requirements for low vulnerability to attack and compromise. Through the implementation of the handshake routine between the central processor and the entrance control, the vulnerability to the development of a universal BAS key has been significantly reduced. It precludes the use of one BAS to defeat any other BAS. Additionally, the system provides the user with a high degree of flexibility in the way the system is utilized, yet the probability of creating false alarms has been reduced through a number of methods. One of the methods is simply the incorporation of the entrance control into the system. The entrance control provides a very positive lockout feature which precludes the user from walking into his armed system. In addition, the logic employed at the central processor will not allow the user to arm his system in various operational modes which may lead to false alarm conditions. The system also provides the user with a continuous analysis of the operability of the system, i. e., if trouble occurs within the system the user is alerted to that trouble and the trouble condition itself is displayed to him in the form of a two-digit code at the central processor. These relatively sophisticated features can be provided cost-effectively through the use of microprocessors and large scale integration. The BAS Phase I Report concluded that the original cost goals could be met and that conclusion is still maintained to be viable.

BAS feasibility has been demonstrated through the development of the two deliverable breadboard systems. It is therefore recommended that a seven step program be undertaken to further develop the BAS. The following work statements are arranged in chronological order.

1. Conduct a partial productization of the BAS to allow a cost effective quantity build for large scale testing.

2. Fabricate the test systems while determining all test parameters, reporting methods, selection of test sites, data recording and analysis, etc.

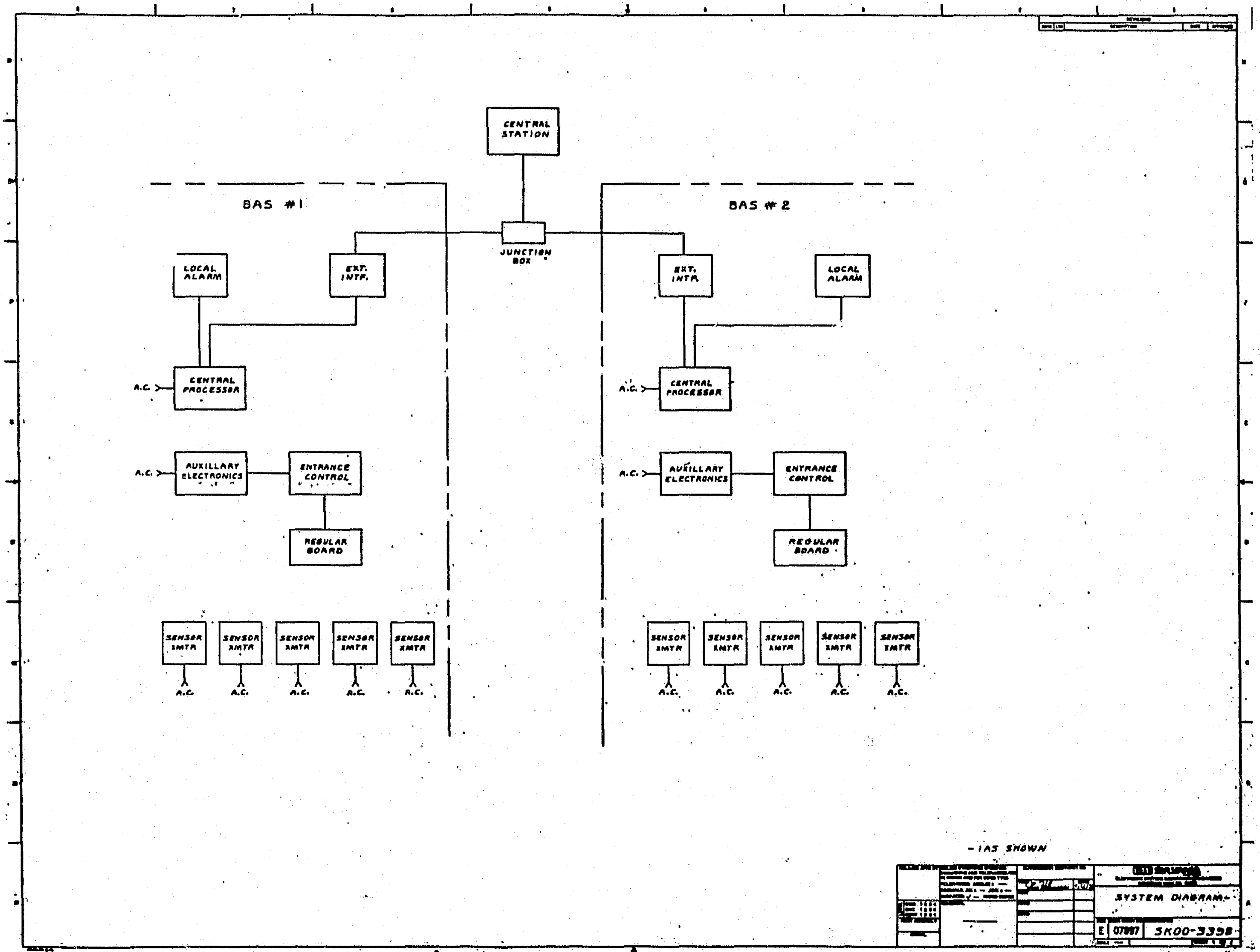
3. Conduct large scale field tests.

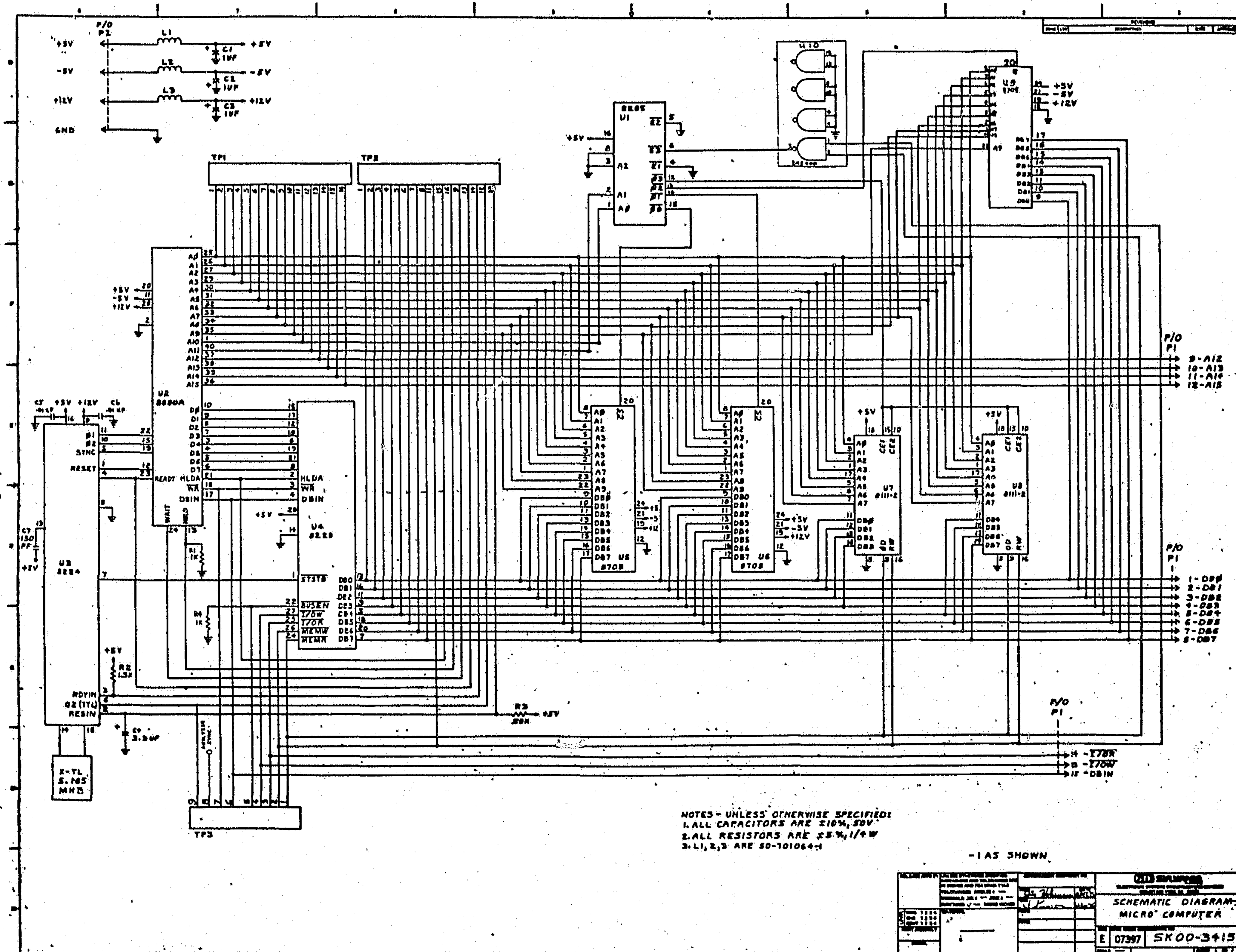
4. Analyze the results and make modification recommendations if required.
5. Modify the systems as required.
6. Complete the BAS productization.
7. Transfer the acquired technology to manufacturers who wish to market this system.

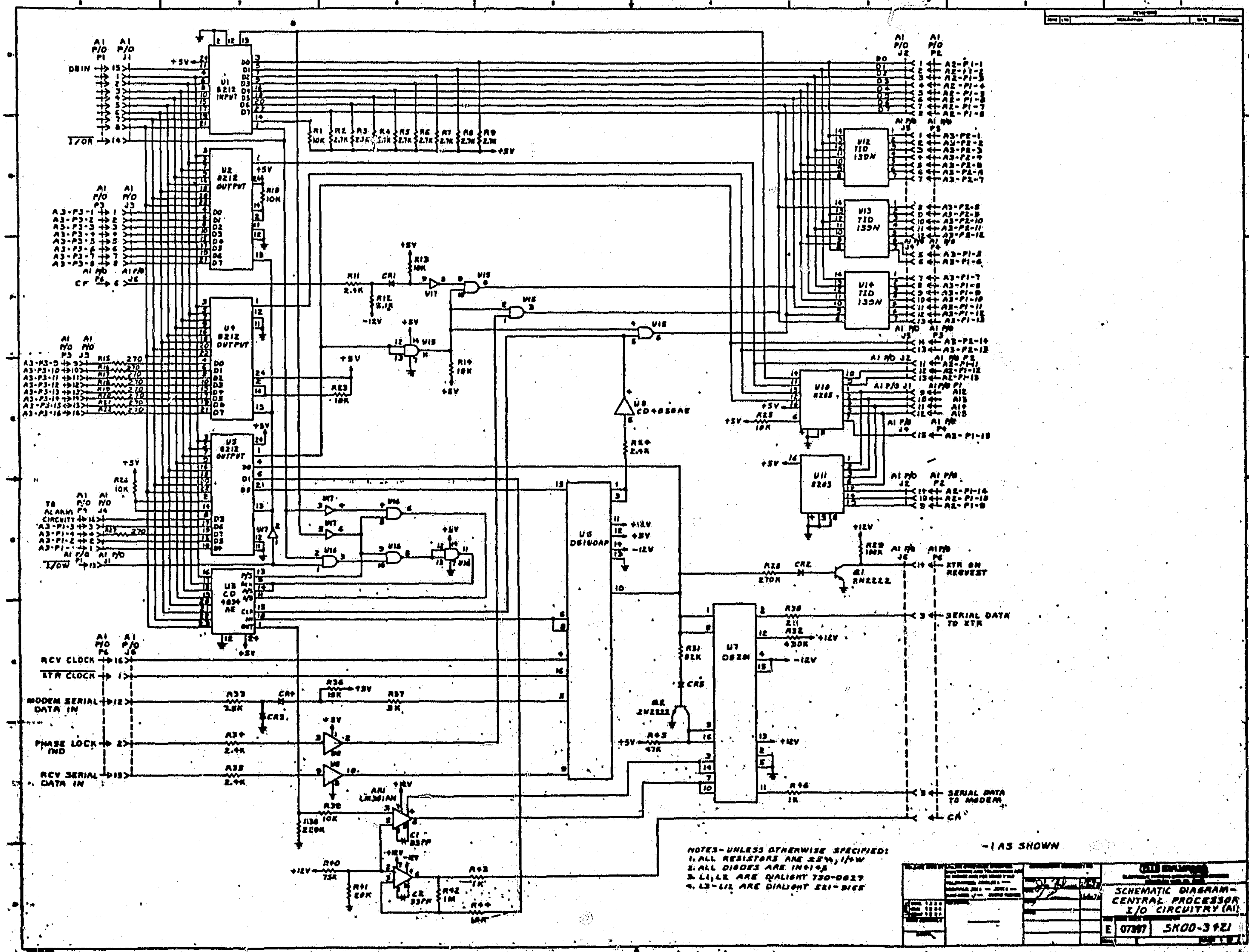
It is estimated that such a program would take two to three years to implement.

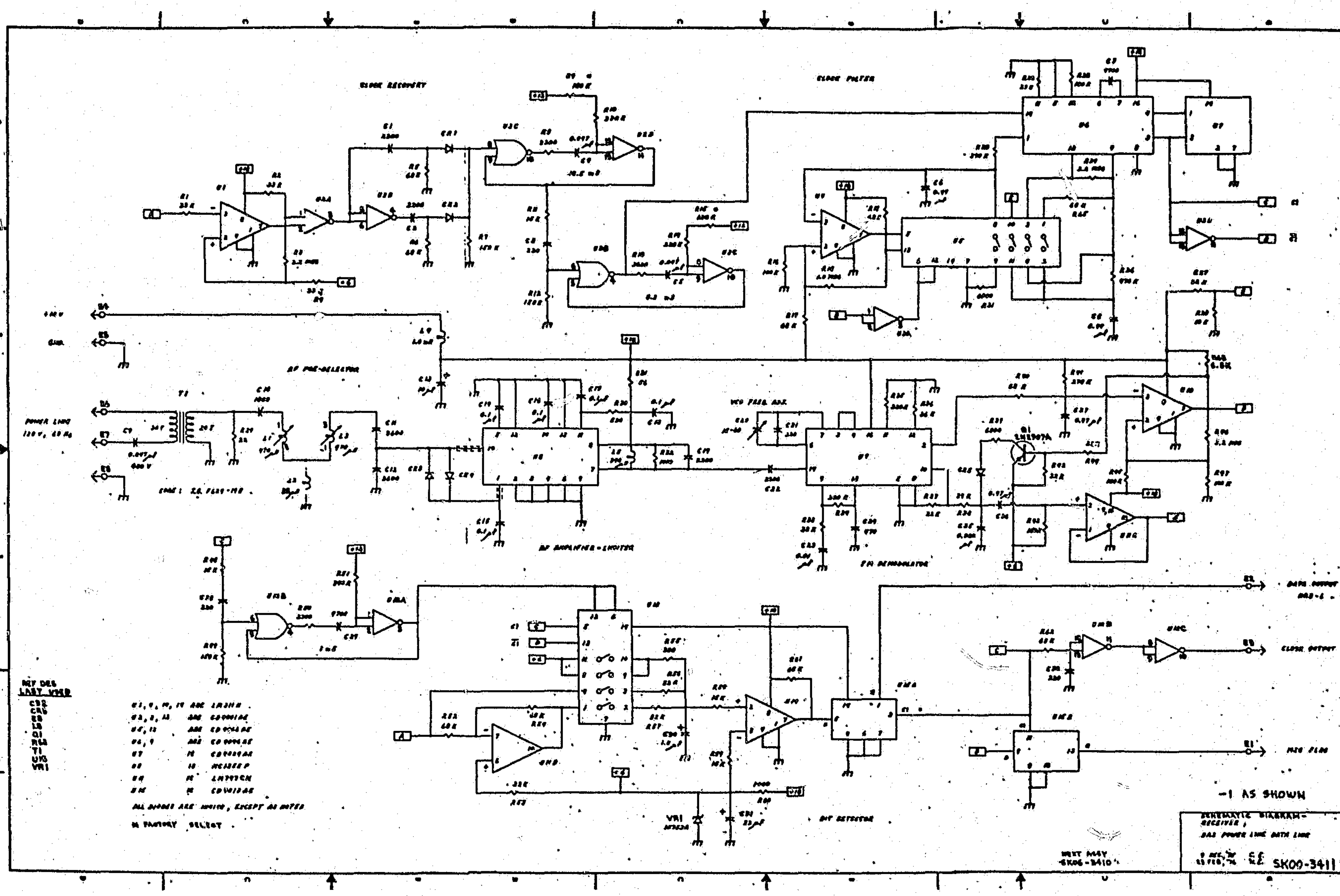
Appendix A

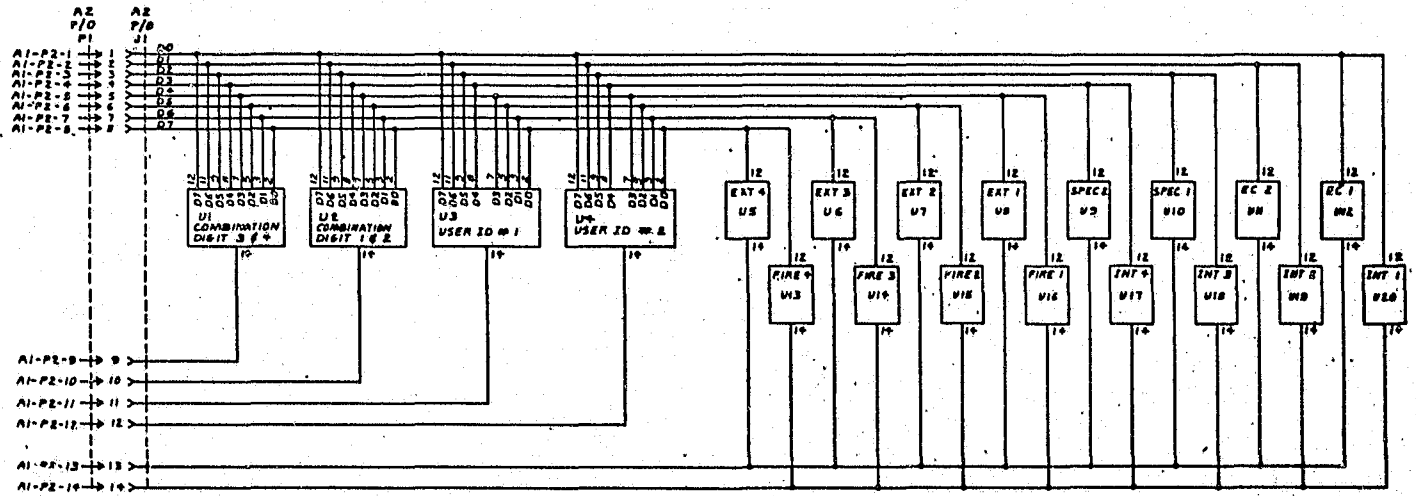
BAS SCHEMATIC DIAGRAMS AND PART LISTS


CENTRAL STATION
BAS #1
BAS # 2
JUNCTION BOX
LOCAL ALARM
EXT. INTF.
CENTRAL PROCESSOR
A.C.
AUXILLARY ELECTRONICS
ENTRANCE CONTROL
REGULAR BOARD
SENSOR XMTR
-1AS SHOWN
SYSTEM DIAGRAM
E
SK00-3398


NOTES - UNLESS OTHERWISE SPECIFIED:
1. ALL CAPACITORS ARE ±10%, 50V
2. ALL RESISTORS ARE ±5%, 1/4W
3. L1, 2, 3 ARE 50-701064-1
-1 AS SHOWN
SCHEMATIC DIAGRAM MICRO COMPUTER
E 07397 SK00-3415


NOTES- UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS ARE ±5%, 1/4W
2. ALL DIODES ARE IN914B
-1 AS SHOWN
SCHEMATIC DIAGRAM-
CENTRAL PROCESSOR
I/O CIRCUITRY (A1)
E
07397
SK00-3421


-1 AS SHOWN
SK00-3411

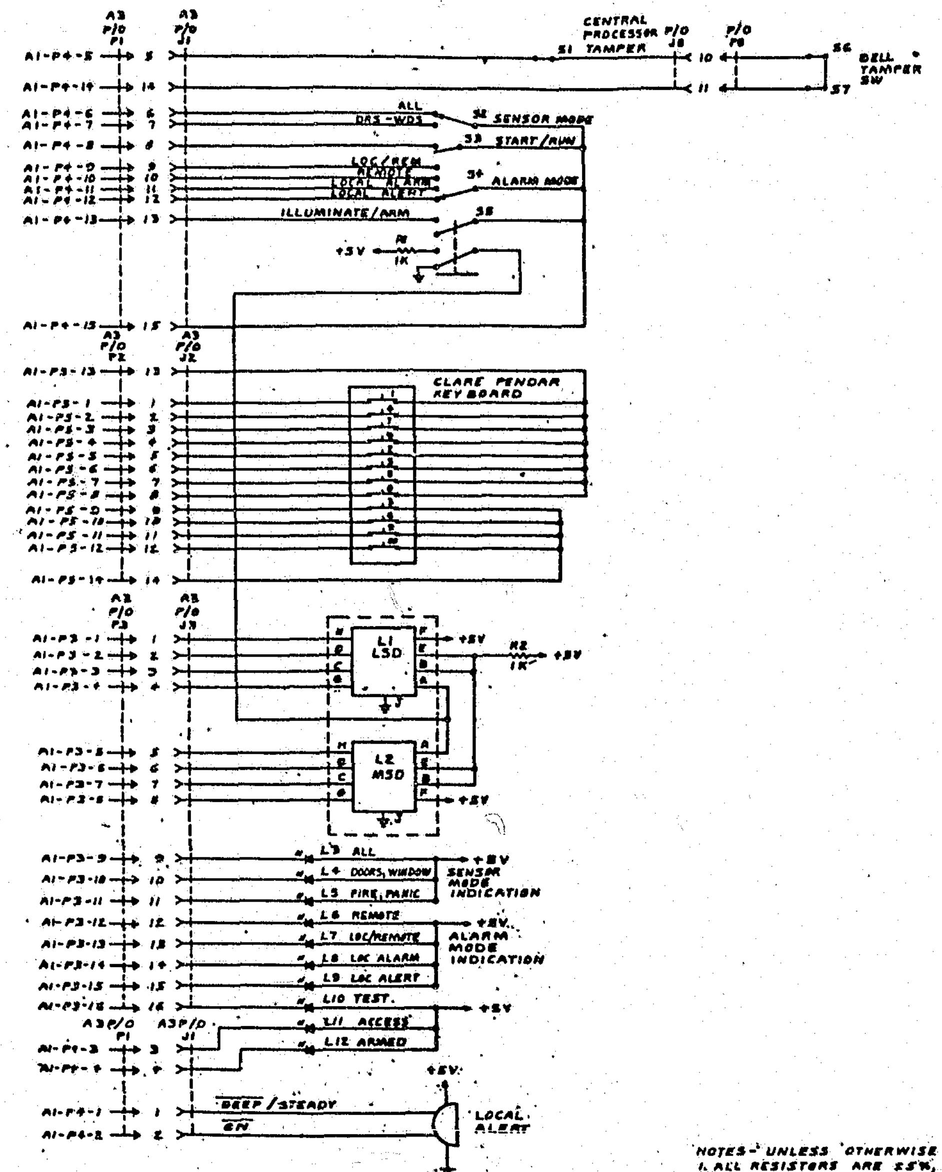


NOTES- UNLESS OTHERWISE SPECIFIED:
1. ALL I.C. ARE TID121

-1 AS SHOWN

SCHEMATIC DIAGRAM-CODE PLUG BOARD (A2)

E 07387 SK00-3420

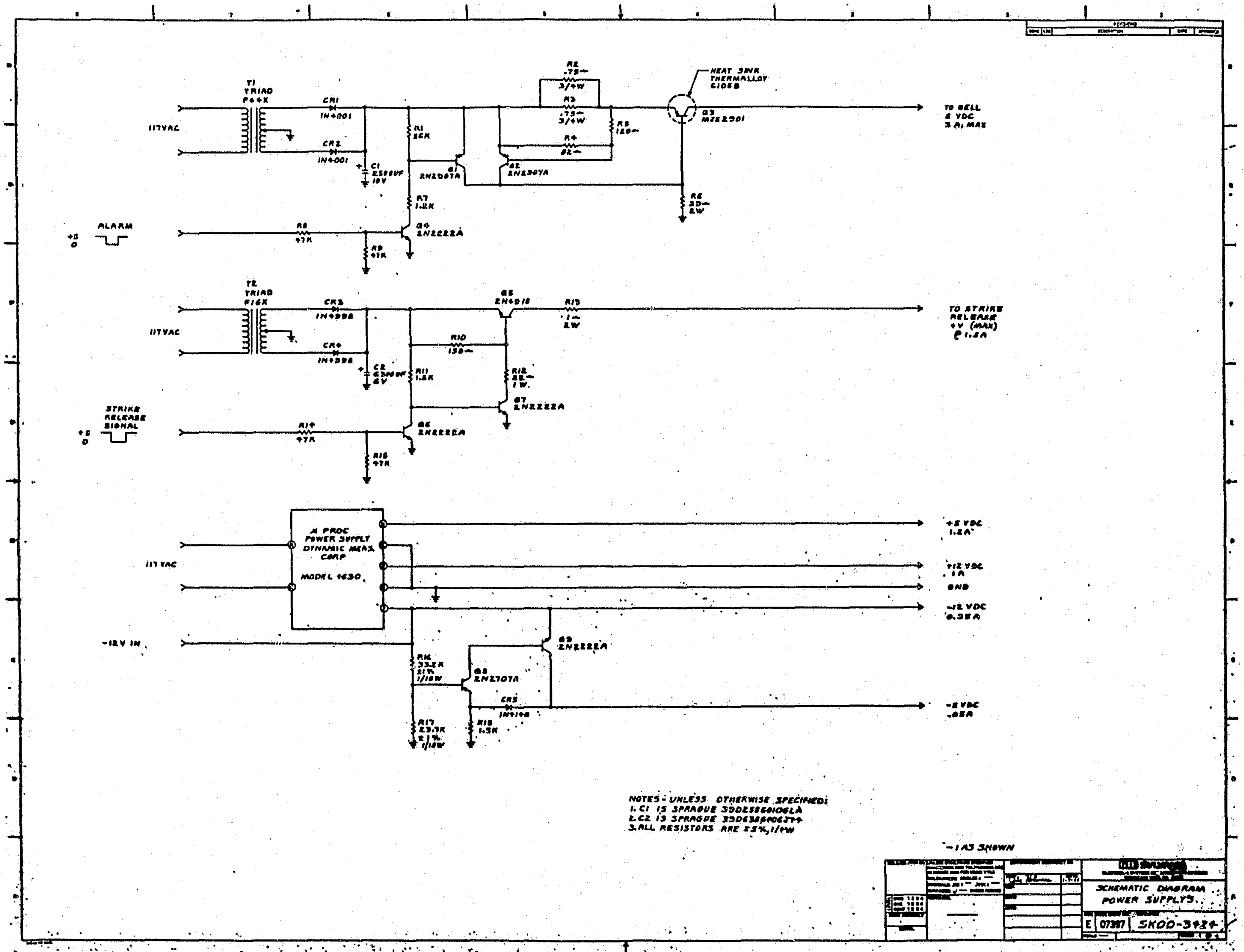


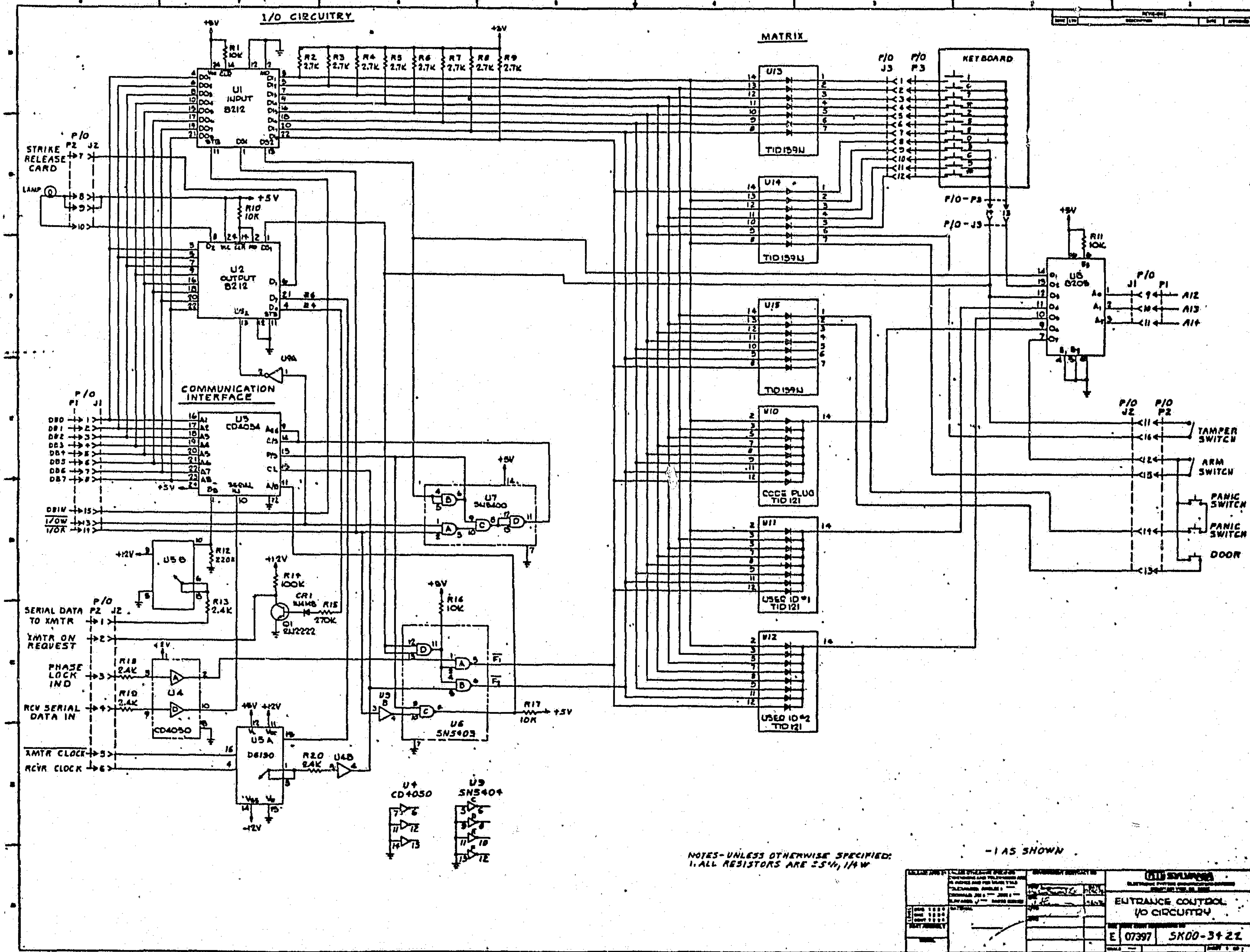
NOTES- UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS ARE ±5%, 1/4W
2. L1, L2 ARE DIALIGHT 739-0207-001
3. L3-L10 ARE DIALIGHT 521-9189
4. L11 IS DIALIGHT 521-9165
5. L12 IS DIALIGHT 249-7868-3331-504

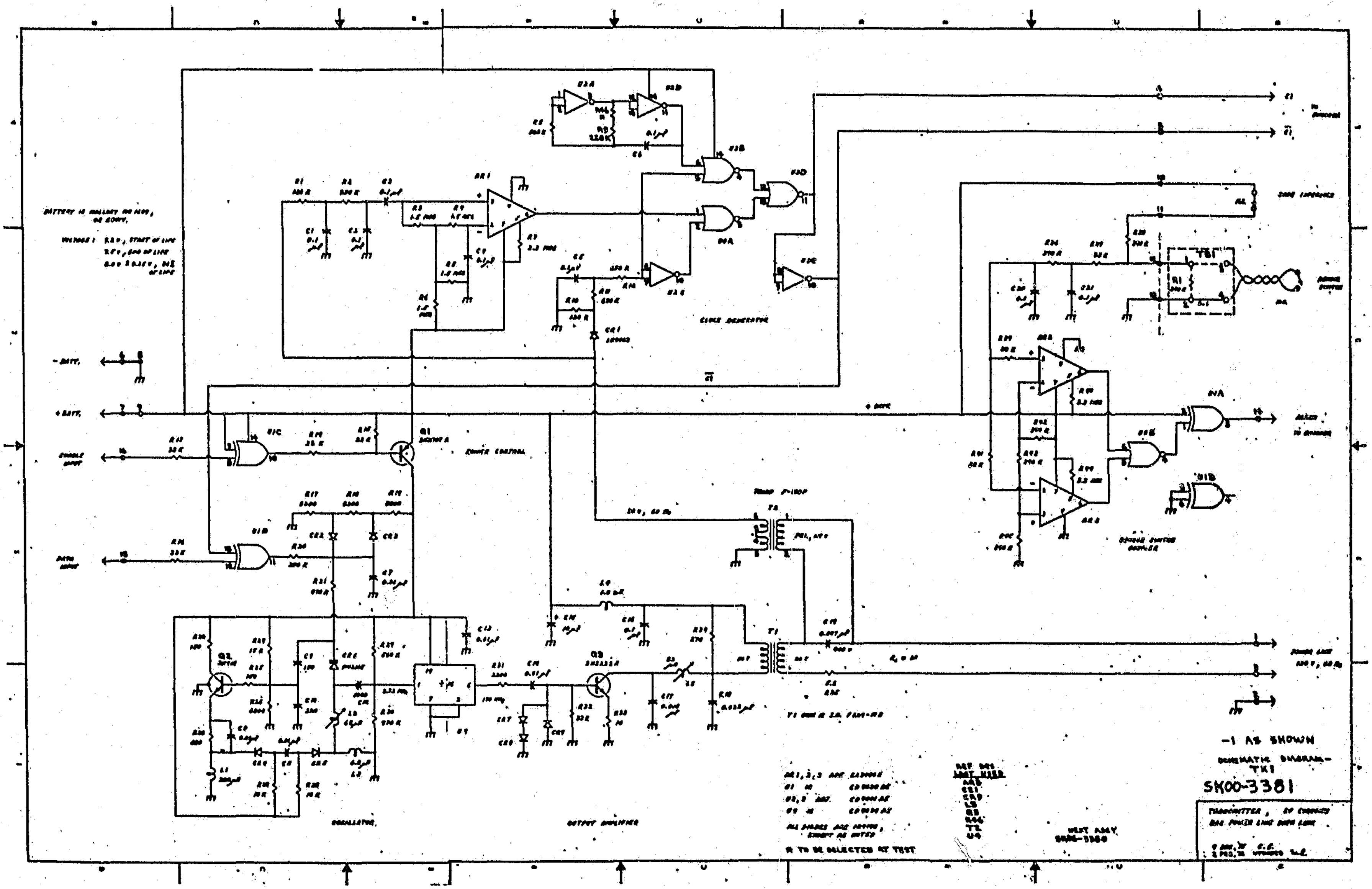
- 1 AS SHOWN -

SCHEMATIC DIAGRAM - FRONT - PANEL (A3)

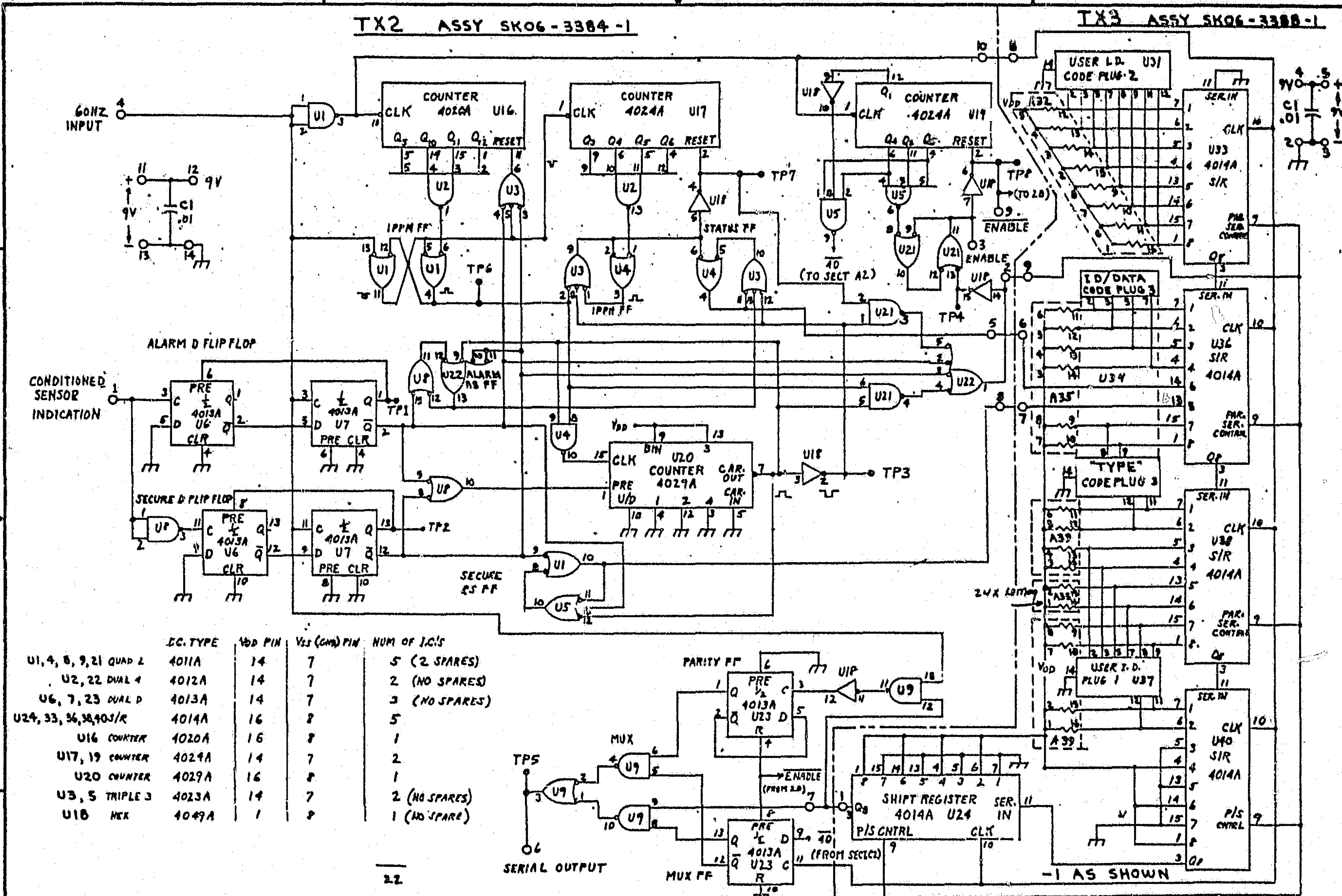
E 07397 5K00-3419


T1 TRIAD F44X
117VAC
CR1 1N4001
CR2 1N4001
C1 2500UF 10V
R1 56K
R2 .75Ω 3/4W
R3 .75Ω 3/4W
R4 82Ω
R5 120Ω
HEAT SINK THERMALLOY 6106B
Q3 MJE2901
TO BELL 5 VDC 3 A, MAX
Q1 2N2907A
Q2 2N2904A
R6 35Ω 2W
R7 1.2K
ALARM
R8 47K
R9 47K
Q4 2N2222A
T2 TRIAD F16X
117VAC
CR3 1N4998
CR4 1N4998
C2 6300UF 6V
Q5 2N4918
R13 1Ω 2W
TO STRIKE RELEASE 4V (MAX) @ 1.5A
R10 130Ω
R11 1.5K
R12 22Ω 1W.
Q7 2N2222A
STRIKE RELEASE SIGNAL
R14 47K
R15 47K
Q6 2N2222A
µ PROC POWER SUPPLY DYNAMIC MEAS. CORP MODEL 4630
117VAC
+5 VDC 1.2A
+12 VDC 1A
GND
-12 VDC 0.35A
-12V IN
Q9 2N2222A
R16 33.2K ±1% 1/10W
Q8 2N2907A
CR5 1N4148
-5 VDC .05A
R17 23.7K ±1% 1/10W
R18 1.5K
NOTES - UNLESS OTHERWISE SPECIFIED:
1. C1 IS SPRAGUE 39D258G010GL4
2. C2 IS SPRAGUE 39D638G006JT4
3. ALL RESISTORS ARE ±5%, 1/4W
-1 AS SHOWN
SCHEMATIC DIAGRAM
POWER SUPPLYS.
E 07387 SKOD-3424


I/O CIRCUITRY
MATRIX
KEYBOARD
U1 INPUT 8212
U2 OUTPUT 8212
COMMUNICATION INTERFACE
U3 CD4034
U7 SN5400
U6 SN5403
U5A D6150
U4 CD4050
U9 SN5404
U8 8205
U13 TID159N
U14 TID159N
U15 TID159N
U10 CODE PLUG TID121
U11 USED ID #1 TID121
U12 USED ID #2 TID121
STRIKE RELEASE CARD
LAMP
SERIAL DATA TO XMTR
XMTR ON REQUEST
PHASE LOCK IND
RCV SERIAL DATA IN
XMTR CLOCK
RCVR CLOCK
TAMPER SWITCH
ARM SWITCH
PANIC SWITCH
PANIC SWITCH
DOOR
NOTES- UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS ARE ±5%, 1/4W
-1 AS SHOWN
ENTRANCE CONTROL I/O CIRCUITRY
E 07397 SK00-3422



-1 AS SHOWN
TK1
SK00-3381
R TO BE SELECTED AT TEST



I.C. TYPE		VDD PIN	VSS (GND) PIN	NUM OF I.C.'S
U1, 4, 8, 9, 21 QUAD 2	4011A	14	7	5 (2 SPARES)
U2, 22 DUAL 4	4012A	14	7	2 (NO SPARES)
U6, 7, 23 DUAL D	4013A	14	7	3 (NO SPARES)
U24, 33, 36, 38, 40 S/R	4014A	16	8	5
U16 COUNTER	4020A	16	8	1
U17, 19 COUNTER	4024A	14	7	2
U20 COUNTER	4029A	16	8	1
U3, 5 TRIPLE 3	4023A	14	7	2 (NO SPARES)
U18 HEX	4049A	1	8	1 (NO SPARE)

SCHEMATIC DRAWING INSTRUCTIONS

MECHANICAL DRAWING INSTRUCTIONS

SPECIAL INSTRUCTIONS:

LTR	DESCRIPTION	DATE	APPROVED
A	ADDED PWR LEADS, TP'S	12-?	RWL
B	ADDED COMP. DESIG. CHANGED 40 DECODER	12-11	RWL
C	UP-DATED NUMBERING TO AGREE WITH PWB	2-11	W.L.

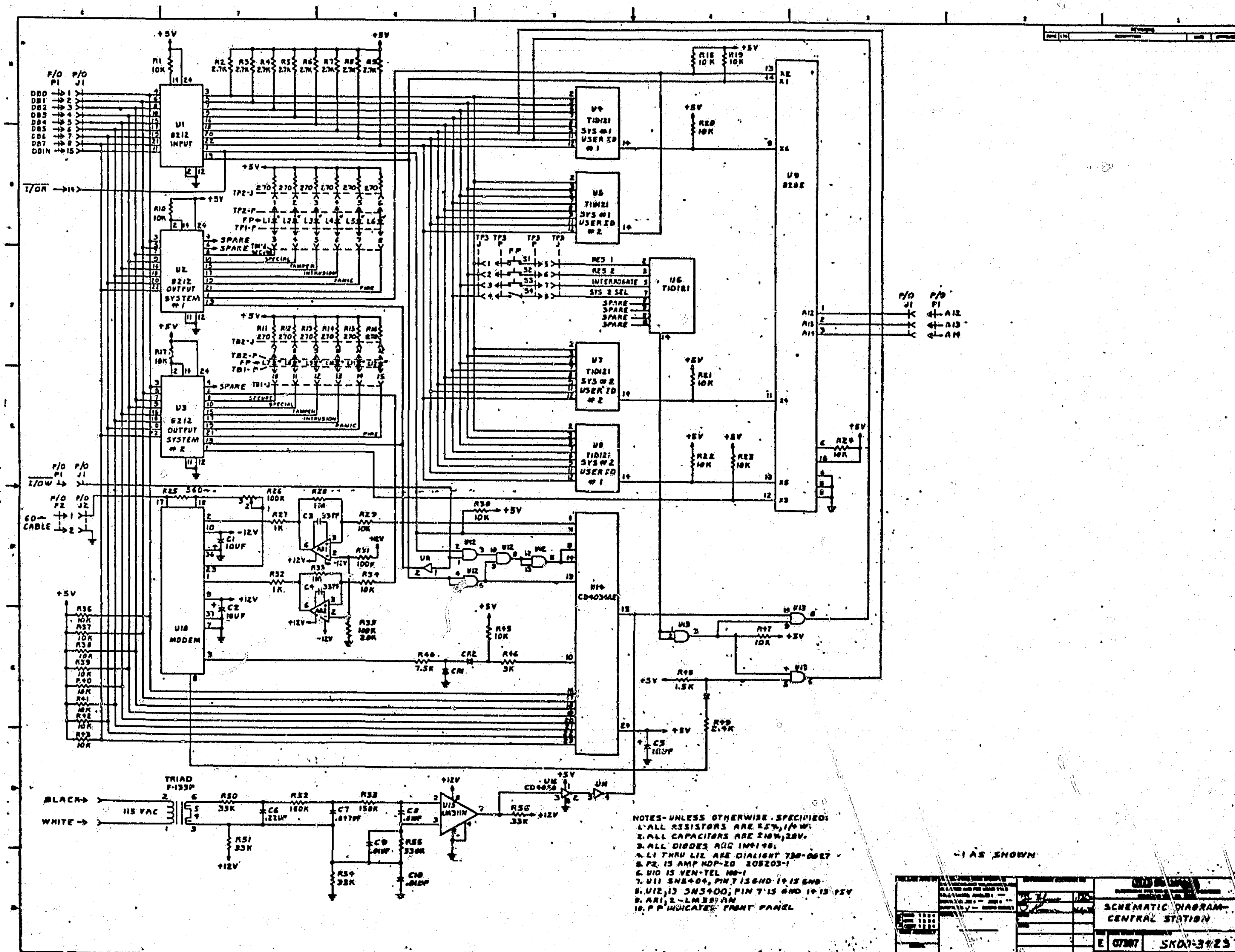
GTE SYLVANIA ELECTRONIC SYSTEMS GROUP — WESTERN DIVISION

TITLE SCHEMATIC DIAGRAM - TRANSMITTER ENCODER

SIZE C | CODE IDENT 07397 | DRAWING NO. SK00-3385 | REV C

SEE ABOVE | SHEET 1 OF 1

ESG-WD-3226 (2-72)



U1 8212 INPUT
U2 8212 OUTPUT SYSTEM #1
U3 8212 OUTPUT SYSTEM #2
U4 TIDI21 SYS #1 USER ID #1
U5 TIDI21 SYS #1 USER ID #2
U6 TIDI21
U7 TIDI21 SYS #2 USER ID #2
U8 TIDI21 SYS #2 USER ID #1
U9 8205
U10 MODEM
U14 CD4036AE
U15 LM311N
TRIAD F-133P
115 VAC
BLACK
WHITE
60-CABLE
SPARE
SPECIAL
TAMPER
INTRUSION
PANIC
FIRE
RES 1
RES 2
INTERROGATE
SYS 2 SEL
NOTES- UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS ARE ±5%, 1/4 W.
2. ALL CAPACITORS ARE ±10%, 25V.
3. ALL DIODES ARE 1N4148.
4. L1 THRU L12 ARE DIALIGHT 739-0927
5. F2, 15 AMP HDP-20 205203-1
6. U10 IS VEN-TEL 100-1
7. U11 SN5404, PIN 7 IS GND 14 IS GND
8. U12, 13 SN5400; PIN 7 IS GND 14 IS +5V
9. AR1, 2 - LM301AN
10. F P INDICATES FRONT PANEL
-1 AS SHOWN
SCHEMATIC DIAGRAM CENTRAL STATION
E
SKD7-3123

NOTES: (UNLESS OTHERWISE SPECIFIED:)

PARTS LIST NO PL SK02-3342

LTR	REVISION DESCRIPTION	DATE	APPROVED

A-13

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42

RECORD OF REVISION STATUS OF EACH SHEET

RELEASE APPD BY

LEVEL
DWG 1 2 3 4
CHK 1 2 3 4
CONT 1 2 3 4

MODEL CP-1

NEXT ASSEMBLY

GOVERNMENT CONTRACT NO

PREP L.F. DATE 2/17/76
CHK
APPD
APPD

GTE SYLVANIA INCORPORATED
ELECTRONIC SYSTEMS GROUP/WESTERN DIVISION
MOUNTAIN VIEW, CA 94042

BAS
PROCESSOR ASSEMBLY

SIZE	CODE IDENT	PARTS LIST NO
A	07397	PL SK02-3342

SHEET 1 OF 4

ESG-1085.8 (1-74)

NOTES: 1. D.M.C.
2. CHERRY SW. CO.
3. DIALIGHT CO.

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
			-1							
			1			SK82-3379-1		ENCLOSURE W/COVER		1
			1			SK82-3343-1		FRONT PANEL		2
			1			SK06-3410		CCA, RECEIVER		3
			1			SK06-		CCA, μ-COMPUTER		4
			1			SK06-		CCA I/O INTERFACE		5
			1			SK06-		CCA BELL CKT		6
			1			SK06-		CCA CODE PLUG		7
			1			4620		POWER SUPPLY	1	8
			1			E63-60H		TAMPER SWITCH	2	9
			1			554-2221		SWITCH, PUSH, MOM (ARM)	3	10
			1			325-0075		PUSHBUTTON CAP, WHITE (5/8" SQ)	3	11

KEY:
*-VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING
F–FEET
I–INCHES
B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL SK02-3342

CODE IDENT 07397 | SHEET 2 | REV

ESG - 1086.8 (1-72)

NOTES: 4. GRAYHILL
5. ROGAN
6. CLARE-PENDAR
7. FLOYD BELL, ASSOC.

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
			-1							
			1			SK06-3380		CCA TRANSMITTER		12
			1			SK82-3414		BRACKET, TXM		13
			1			50A36-01-1-5N		SWITCH, ROTARY, 36°	4	14
			1			50A60-01-1-3N		SWITCH, ROTARY 60°	4	15
			2			RB-67-OP-DCM (1/8" SHAFT)		KNOB, POINTER	5	16
			1			940002 (DRAWING NO.)		KEYBOARD, 12 KEYS	6	17
			1			AL-175		AUDIOLARM	7	18
			8			521-9189		LED, RED — SMALL	3	19
			1			521-9165		LED RED - LARGE (ACCESS)	3	20
			1			730-0027		DUAL READOUT, SOLID STATE	3	21
			1			250-8738-14-504		LAMP HOLDER, LED, SOCKET (ARMED)	3	22

KEY:
*-VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING
F–FEET
I–INCHES
B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL SK02-3342

CODE IDENT 07397 | SHEET 3 | REV

ESG - 1086.8 (1-72)

NOTES: 8. THE HARTWELL CORP
9. TRIAD

QUANTITY REQUIRED			-1	KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
			1			NSG-S3-2		NYLATCH FASTENER - GROMMET (WHITE)	8	23
			1			NSP-S3-3-2		" " PLUNGER (WHITE)	8	24
										25
										26
			1			SK82-3409-1		KEYBOARD HOUSING		27
			1			F-44X		TRANSFORMER	9	28
			10			1435-M03-F05A-440		STANDOFF MALE/FEM 1/2" 440		29
			3			1459 " "	"	" " 1 1/4 -4-40		30
										31
										32
										33

KEY:
*-VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING
F-FEET
I-INCHES
B-BULK
A/R-AS REQUIRED
R-REFERENCE

PL SK02-3342
CODE IDENT 07397 | SHEET 4 | REV

ESG - 1086.8 (1-72)

NOTES: (UNLESS OTHERWISE SPECIFIED:)

PARTS LIST NO PL

LTR	REVISION DESCRIPTION	DATE	APPROVED

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42

RECORD OF REVISION STATUS OF EACH SHEET

RELEASE APPD BY

LEVEL				
DWG	1	2	3	4
CHK	1	2	3	4
CONT	1	2	3	4

MODEL

NEXT ASSEMBLY

GOVERNMENT CONTRACT NO

PREP DATE

CHK

APPD

APPD

GTE SYLVANIA INCORPORATED

ELECTRONIC SYSTEMS GROUP/WESTERN DIVISION
MOUNTAIN VIEW, CA 94042

CENTRAL PROCESSOR
FRONT PANEL

SIZE	CODE IDENT	PARTS LIST NO
A	07397	PL

SHEET 1 OF 3

ESG-1085.8 (1-74)

CONTINUED

2 OF 5

NOTES: 1. DIALCO
2. BELL ALARM
3. CLARE-PENDAR
4 CHERRY E. P.
5. GRAYHILL
6. ARCHER
7. CIRCUIT ASSEMBLY CORP

QUANTITY REQUIRED			-1	KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
			1	R				SCHEMATIC DIAGRAM		1
										2
			2					RESISTOR 1K±5% 1/4W (R1,2)		3
			1			739-0207-601		2 DIGIT LED DISPLAY	1	4
			8			521-9189		LED RED DIFFUSED SMALL	1	5
			1			521-9165		LED RED DIFUSED LARGE	1	6
			1			249-7868-3331-504		LED PANEL MOUNT RED		7
			1			AL-175		LOCAL ALERT	2	8
			1			94002		KEYBOARD	3	9
			1			E63-60H		SWITCH TAMPER (S1)	4	10
			1			50A60-01-1-3N		SWITCH SENSOR MODE (S2)	5	11

KEY:
*-VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING
F-FEET
I-INCHES
B-BULK
A/R-AS REQUIRED
R-REFERENCE

PL

CODE IDENT 07397 | SHEET 2 | REV

ESG - 1086.8 (1-72)

NOTES:

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
			1			275-327		SWITCH START SPST (S3)	6	12
			1			50A36-01-1-5N		SWITCH ALARM MODE (S4)	5	13
			1			554-2221		SWITCH ILLUMINATE/ARM (S5)	1	14
			1			325-0075		CAP (ILLUM/ARM SWITCH)	1	15
			2			501-0700-005		CONNECTOR	1	16
			2			CAS-16P01-26-1-T0-024		DIP INTERCONNECT CABLE 16 PIN	7	17
			1			CAS-14P01-26-1-T0-018		DIP INTERCONNECT CABLE 14 PIN		18
										19
										20
										21
										22

KEY:
*-VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F–FEET
I–INCHES

B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL

CODE IDENT 07397 | SHEET 3 | REV

ESG - 1086.8 (1-72)

NOTES: (UNLESS OTHERWISE SPECIFIED:)

PARTS LIST NO PL

LTR	REVISION DESCRIPTION	DATE	APPROVED

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42

RECORD OF REVISION STATUS OF EACH SHEET

RELEASE APPD BY

LEVEL

DWG	1	2	3	4
CHK	1	2	3	4
CONT	1	2	3	4

MODEL

NEXT ASSEMBLY

GOVERNMENT CONTRACT NO

PREP DATE

CHK

APPD

APPD

GTE SYLVANIA INCORPORATED
ELECTRONIC SYSTEMS GROUP/WESTERN DIVISION
MOUNTAIN VIEW, CA 94042

MICRO COMPUTER ASSY-
BURGLARY ALARM SYSTEM

SIZE	CODE IDENT	PARTS LIST NO
A	07397	PL

SHEET 1 OF 4

ESG-1085.8 (1-74)

NOTES:

QUANTITY REQUIRED -3	-2	-1	KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
		1	R				SCHEMATIC DIAGRAM		1
									2
	1	1			SK06-3414		PRINTED WIRING BOARD		3
									4
									5
									6
3	3	3			CSR13G105K	M39003-01-2356	CAPACITOR 1µF TANTALUM 50V (C1,2,3)		7
1	1	1					CAPACITOR µF TANTALUM (C4)		8
2	2	2			CK06104K	M39014-02-1218	CAPACITOR .01µF (C5,6)		9
1	1	1			CMR05F151J0DL		CAPACITOR 150 PF (C7)		10
2	2	2					RESISTOR 1K ±5% 1/4W (R1,4)		11

KEY:
*-VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING
F–FEET
I–INCHES
B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL

CODE IDENT 07397 | SHEET 2 | REV

ESG - 1086.8 (1-72)

NOTES:

QUANTITY REQUIRED	-3	-2	-1	KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
	1	1	1					RESISTOR 1.5K ±5% 1/4W		12
								(R2)		
	1	1	1					RESISTOR 50K ±5% 1/4W		13
								(R3)		
	1	1	1			8205		I.C. 1 of 8 DECODER		14
								(U1)		
	1	1	1			8080A		I.C. MICRO-PROCESSOR		15
								(U2)		
	1	1	1			8224		I.C. CLOCK GENORATOR		16
								(U3)		
	1	1	1			8228		I.C. SYS. CONTROLLER + BUS		17
								DRIVER (U4)		
	1	2	3			8708		I.C. PROM 1K x 8		18
								(U 5, 6, 9)		
	2	2	2			8111-2		I.C. 256 x 4 RAM		19
								(U7, 8)		
	1	1	1			SN5400	15-823114-1	I.C. QUAD 2-INPUT NAND		20
								GATE (U10)		
	1	1	1					CRYSTAL 5.185 MHz		21
								(X-TAL)		
	3	3	3				50-701064-1	INDUCTOR (FERRITE)		22

KEY:
*-VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F–FEET
I–INCHES

B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL

CODE IDENT 07397 | SHEET 3 | REV

ESG - 1066.8 (1-72)

NOTES:

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
		-2	-1							
		2	2			514-AG11D	72-701080-3	SOCKET 14 PIN LOW PRO-FILE		23
		4	4			516-AG11D	72-701080-1	SOCKET 16 PIN LOW PROFILE		24
		2	2			518-AG11D		SOCKET 18 PIN L.P.		25
		3	3			524-AG11D	72-701080-4	SOCKET 24 PIN L.P.		26
		1	1			528-AG11D		SOCKET 28 PIN L.P.		27
		1	1			540-AG10D		SOCKET 40 PIN L.P.		28

KEY:
*-VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F–FEET
I–INCHES

B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL

CODE IDENT 07397 | SHEET 4 | REV

ESG - 1086.8 (1-72)

NOTES: (UNLESS OTHERWISE SPECIFIED:)

PARTS LIST NO PL

LTR	REVISION DESCRIPTION	DATE	APPROVED

A-24

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42

RECORD OF REVISION STATUS OF EACH SHEET

RELEASE APPD BY

LEVEL
DWG 1 2 3 4
CHK 1 2 3 4
CONT 1 2 3 4

MODEL

NEXT ASSEMBLY

GOVERNMENT CONTRACT NO

PREP DATE
CHK
APPD
APPD

GTE SYLVANIA INCORPORATED
ELECTRONIC SYSTEMS GROUP/WESTERN DIVISION
MOUNTAIN VIEW, CA 94042

CENTRAL PROCESSOR
I/O CIRCUITRY

SIZE	CODE IDENT	PARTS LIST NO
A	07397	PL

SHEET 1 OF 5

ESG-1085.8 (1-74)

NOTES:

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
			-1							
			1	R				SCEMATIC DIAGRAM		1
			10					RESISTOR 10K ±5% 1/4W		2
								(R1,10,13,14,23,25,26,36,39,44)		
			8					RESISTOR 2.7K ±5% 1/4W		3
								(R2-9)		
			4					RESISTOR 2.4K ±5% 1/4W		4
								(R11,24,34,35)		
			1					RESISTOR 5.1K ±5% 1/4W		5
								(R12)		
			9					RESISTOR 270 ±5% 1/4W		6
								(R15-22,27)		
			1					RESISTOR 270K ±5% 1/4W		7
								(R28)		
			1					RESISTOR 100K ±5% 1/4W		8
								(R29)		
			1					RESISTOR 2K ±5% 1/4W		9
								(R30)		
			1					RESISTOR 82K ±5% 1/4W		10
								(R31)		
			1					RESISTOR 430K ±5% 1/4W		11
								(R32)		

KEY:
*-VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F-FEET
I-INCHES

B-BULK
A/R-AS REQUIRED
R-REFERENCE

PL

CODE IDENT 07397 | SHEET 2 | REV

ESG - 1086.8 (1-72)

NOTES:

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
			-1							
			1					RESISTOR 7.5K ±5% 1/4W		12
								(R33)		
			1					RESISTOR 3K±5% 1/4W		13
								(R37)		
			1					RESISTOR 220K ±5% 1/4W		14
								(R38)		
			1					RESISTOR 75K ±5% 1/4W		15
								(R40)		
			1					RESISTOR 20K±5% 1/4W		16
								(R41)		
			1					RESISTOR 1M ±5% 1/4W		17
								(R42)		
			2					RESISTOR 1K ±5% 1/4W		18
								(R43, 46)		
			1					RESISTOR 47K±5% 1/4W		19
								(R45)		
										20
			2			CMR05E330J0DL		CAPACITOR 33 PF 500V		21
								(C1, 2)		
			3			CSR13G105K		CAPACITOR 1MF 50VDC		22
								(C3,4,5)		

KEY:
* -VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F–FEET
I–INCHES

B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL

CODE IDENT 07397 | SHEET 3 | REV

ESG - 1086.8 (1-72)

NOTES:

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
			-1							
			2			LM301AN		OPERATIONAL AMPLIFIER		23
								(AR1, 2)		
			4			8212		I/O PORT (8 BIT)		24
								(U1, 2, 4, 5)		
			1			CD4034AE		I/O REGISTAR		25
								(U3)		
			1			DG190AP		ANALOG SWITCH		26
								(U6)		
			1			DG201		ANALOG SWITCH		27
								(U7)		
			1			CD4050AE		HEX BUFFER		28
								(U8)		
			2			8205		1 OF 8 DECODER		29
								(U10, 11)		
			3			TID139N		DIODE ARRAY		30
								(U12, 13, 14)		
			1			SN5403		QUAD 2-INPUT NAND (OC)		31
								(U15)		
			1			SN5400		QUAD 2-INPUT NAND		32
								(U16)		
			1			SN5404		HEX INVERTER		33
								(U17)		

KEY:
* -VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F—FEET
I—INCHES

B—BULK
A/R—AS REQUIRED
R—REFERENCE

PL

CODE IDENT 07397 | SHEET 4 | REV

ESG - 1086.8 (1-72)

NOTES:

QUANTITY REQUIRED			-1	KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
			2			2N2222		TRANSISTOR NPN		34
								(Q1, 2)		
			5			1N4148		DIODE		35
								(CR1, 2, 3, 4, 5)		
			3				50-701064-1	FERRITE INDUCTOR (L1, 2, 3)		36
			11				72-701074-1	DIP SOCKET (WIRE WRAP) 14		37
								PIN		
			12				72-701074-2	DIP SOCKET (WW) 16 PIN		38
			5				72-701074-3	DIP SOCKET (WW) 24 PIN		39
			3				72-701075-1	COMPONENT CARRIER		40
								14 PIN		
			1				72-701075-2	COMPONENT CARRIER		41
								16 PIN		
			1					VECTORBOARD P-PATTERN		42
								(3.25" x 10.5")		
										43
										44

KEY:
* -VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F–FEET
I–INCHES

B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL

CODE IDENT 07397 | SHEET 5 | REV

ESG - 1086.8 (1-72)

NOTES:

BAS DATA LINK RECEIVER 18 DEC, 75

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
					C1			CAPACITOR, CERAMIC, 2200 pf, 200 V		
					C2			CAP, CER, 2200 pf, 200 V		
					C3			CAP, CER, 220 pf, 200 V		
					C4			CAP, MYLAR, 0.047 μf ± 10%, 80 V		✓
					C5			CAP, MYLAR, 0.047 μf ± 10%, 80 V		✓
					C6			CAP, CER, 0.47 μf, 50 V		
					C7			CAP, MYLAR, 4700 pf ± 10%, 80 V		✓
					C8			CAP, CER, 0.47 μf, 50 V		
					C9			CAP, MYLAR, 0.047 μf ±10%, 600 V		✓

KEY:
* VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F–FEET
I–INCHES

B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL

CODE IDENT 07397 | SHEET 1 | REV

ESG - 1086.8 (1-72)

NOTES:

BAS DATA LINK RECEIVER 18 DEC., '75

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
					C 10			CAP., MICA, 1800 pf ± 5% DM 19-182-J		✓
					C 11			CAP., MICA, 3600 pf ± 5% DM 19-362-J.		✓
					C 12			CAP., MICA, 3600 pf ± 5% DM 19-362-J		✓
					C 13			CAP., ELECTROLYTIC, TANTALUM, 10 µf, 20 V		
					C 14			CAP., CER., 0.1 µf, 50 V		
					C 15			CAP., CER., 0.1 µf, 50 V		
					C 16			CAP., CER., 0.1 µf, 50 V		
					C 17			CAP., CER., 0.1 µf, 50 V		
					C 18			CAP., CER., 0.1 µf, 50 V		
					C 19			CAP., MICA, 2200 pf ± 5%		✓
					C 20			CAP., VAR., 15 TO 60 pf ERIE 538-011F-15-60		✓

KEY:
* VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F–FEET
I–INCHES

B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL

CODE IDENT 07397 SHEET 2 REV

ESG - 1086.8 (1-72)

NOTES:

BAS DATA LINK RECEIVER 18 DEC., '75

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
					C 21			CAP, MICA, 220 pf ± 5%		✓
								CMR05F221 JODL STORES		
					C 22			CAP, CER, 2200 pf, 200 V		
					C 23			CAP, CER, 0.01 μf ± 10%		
					C 24			CAP, CER, 470 pf, 200 V		
					C 25			CAP, CER, 0.022 μf, 200 V		
					C 26			CAP, CER, 0.47 μf, 50 V		
					C 27			CAP, CER, 0.47 μf, 50 V		
					C 28			CAP, CER, 220 pf, 200 V		
					C 29			CAP, CER, 4700 pf, 200 V		
					C 30			CAP, ELECTROLYTIC, TANT, 1.0 μf, 35 V		
					C 31			CAP, ELECTROLYTIC, TANT, 22 μf, 15 V		

KEY:
* - VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F—FEET
I—INCHES

B—BULK
A/R—AS REQUIRED
R—REFERENCE

PL

CODE IDENT 07397 | SHEET 3 | REV

ESG - 1086.8 (1-72)

NOTES:

BAS DATA LINK RECEIVER 18 DEC., '75

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
					C 32			CAP., CER., 220 pf, 200 V		
					CR 1			DIODE, 1N4148		
					CR 2			DIODE, 1N4148		
					CR 3			DIODE, 1N4148		
					CR 4			DIODE, 1N4148		
					CR 5			DIODE, 1N4148		
					CR 6			DIODE, 1N753 A		
					L 1			INDUCTOR, VAR., 470 μH		✓
								CAMBION 7106-26		
					L 2			INDUCTOR, 33 ~~36~~ μH ± 10 %		
								MS 75089-5		✓

KEY:
*-VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING
F–FEET
I–INCHES
B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL

CODE IDENT 07397 | SHEET 4 | REV

ESG-1086.8 (1-72)

NOTES:

BAS DATA LINK RECEIVER 18 DEC., '75

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
					L3			INDUCTOR, VAR., 470 μH		
								CAMBION 7106-26		✓
					L4			IND., 1.0 mH ± 10%		
								MS 75089-23		
					L5			IND., 390 μH ± 10%		
								MS 75089-18		
					L6, 7			CORE, FERRITE, PARASITIC SUPPRESOR,		
								FERROXCUBE PN 56 590 65/4A		
					R1			RESISTOR, 33 K ± 5%		
					R2			RES., 33 K ± 5%		
					R3			RES., 2.2 MEG ± 5%		
					R4			RES., 33 K ± 5%		
					R5			RES., 68 K ± 5%		
					R6			RES., 68 K ± 5%		
					R7			RES., 150 K ± 5%		

KEY:
* - VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F—FEET
I—INCHES

B—BULK
A/R—AS REQUIRED
R—REFERENCE

PL

CODE IDENT 07397	SHEET 5	REV

ESG - 1086.8 (1-72)

NOTES:

BAS DATA LINK RECEIVER

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
					R8			RES., 2200 ± 5 %		
					R9			RES., 180 K ± 5%, SELECTED IN TEST		
					R10			RES., 330 K ± 5%		
					R11			RES., 15 K ± 5 %		
					R12			RES., 150 K ± 5%		
					R13			RES., 2200 ± 5%		
					R14			RES., 220 K ± 5%		
					R15			RES., 120 K ± 5%, SELECTED IN TEST		
					R16			RES., 100 K ± 5 %		
					R17			RES., 68 K ± 5 %		
					R18			RES., 1.0 MEG. ± 5 %		

KEY:
* -VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F–FEET
I–INCHES

B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL

CODE IDENT 07397 | SHEET 6 | REV

ESG - 1086.8 (1-72)

NOTES:

BAS DATA LINK RECEIVER 18 DEC., '75

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
					R 19			RES., 68 K ± 5 %		
					R 20			RES., 390 K ± 5 %		
					R 21			RES., 6800 ± 5 %		
					R 22			RES., 27 K ± 5 %		
					R 23			RES., 180 K ± 5 %		
					R 24			RES., 2.2 MEG. ± 5 %		
					R 25			RES., 68 K ± 5 %		
					R 26			RES., 470 K ± 5 %		
					R 27			RES., 22 K ± 5 %		
					R 28			RES., 10 K ± 5 %		
					R 29			RES., 22 ± 5 %		

KEY:
* VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F–FEET
I–INCHES

B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL

CODE IDENT 07397 | SHEET 7 | REV

ESG - 1086.8 (1-72)

NOTES:

BAS DATA LINK RECEIVER 19 DEC., '75

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
					R30			RES., 820 ±5%		
					R31			RES., 56 ±5%		
					R32			RES., 1000 ±5%		
					R33			RES., 33 K ±5%		
					R34			RES., 220 K ±5%		
					R35			RES., 220 K ±5%		
					R36			RES., 36 K ±5%		
					R37			RES., 22 K ±5%		
					R38			RES., 39 K ±5%		
					R39			RES., 6800 ±5%		
					R40			RES., 68 K ±5%		

KEY:
*-VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING
F–FEET
I–INCHES
B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL

CODE IDENT 07397 | SHEET 8 | REV

ESG - 1086.8 (1-72)

NOTES:

BAS DATA LINK RECEIVER 17 DEC., '75

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
					R 41			RES., 270 K ± 5%		
					R 42			RES., 22 K ± 5%		
					R 43			RES., 150 K ± 5%		
					R 44			RES., 22 K ± 5%		
					R 45			RES., 100 K ± 5%		
					R 46			RES., 2.2 MEG. ± 5%		
					R 47			RES., 100 K ± 5%		
					R 48			RES., 15 K ± 5%		
					R 49			RES., 150 K ± 5%		
					R 50			RES., 2200 ± 5%		
					R 51			RES., 390 K ± 5%		

KEY:
* - VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING
F—FEET
I—INCHES
B—BULK
A/R—AS REQUIRED
R—REFERENCE

PL

CODE IDENT 07397 SHEET 7 REV

ESG - 1086.8 (1-72)

NOTES:

BAS DATA LINK RECEIVER 19 DEC, 75

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
					R 52			RES., 68 K ± 5 %		
					R 53			RES., 33 K ± 5 %		
					R 54			RES., 68 K ± 5 %		
					R 55			RES., 330 ± 5 %		
					R 56			RES., 82 K ± 5 %		
					R 57			RES., 82 K ± 5 %		
					R 58			RES., 15 K ± 5 %		
					R 59			RES., 15 K ± 5 %		
					R 60			RES., 1000 ± 5 % 1/4 W		
					R 61			RES., 68 K ± 5 %		
					R 62			RES., 68 K ± 5 %		

KEY:
* VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F–FEET
I–INCHES

B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL

CODE IDENT 07397 | SHEET 10 | REV

ESG - 1086.8 (1-72)

NOTES:

BAS DATA LINK RECEIVER   19 DEC., '75

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
					T1			TRANSFORMER, CORE: INDIANA GENERAL		✓
								(SYL. BUILD) F624-19H		
					U1			I.C., LM 311 N		
					U2			I.C., CD 4001 AE		
					U3			I.C., CD 4001 AE		
					U4			I.C., LM 311 N		
					U5			I.C., CD 4066 AE		
					U6			I.C., CD 4046 AE		
					U7			I.C., CD 4024 AE		
					U8			I.C., MC 1355 P		

KEY:
* - VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F–FEET
I–INCHES

B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL

CODE IDENT 07397 | SHEET 11 | REV

ESG - 1086.8 (1-72)

NOTES:

BAS DATA LINK RECEIVER 19 DEC. '75

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
					U9			I.C., CD 4046 AE		
					U10			I.C., LM 311 N		
					U11			I.C., LM 747 N		
					U12			I.C., CD 4001 AE		
					U13			I.C., CD 4066 AE		
					U14			I.C., LM 311 N		
					U15			I.C., CD 4013 AE		

KEY:
* VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F–FEET
I–INCHES

B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL

CODE IDENT 07397 | SHEET 12 | REV

ESG - 1086.8 (1-72)

NOTES: (UNLESS OTHERWISE SPECIFIED:)

PARTS LIST NO PL

LTR	REVISION DESCRIPTION	DATE	APPROVED

A-41

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42

RECORD OF REVISION STATUS OF EACH SHEET

RELEASE APPD BY

LEVEL
DWG 1 2 3 4
CHK 1 2 3 4
CONT 1 2 3 4

MODEL

NEXT ASSEMBLY

GOVERNMENT CONTRACT NO

PREP DATE

CHK

APPD

APPD

GTE SYLVANIA INCORPORATED
ELECTRONIC SYSTEMS GROUP/WESTERN DIVISION
MOUNTAIN VIEW, CA 94042

CENTRAL PROCESSOR
CODE PLUG BOARD

SIZE	CODE IDENT	PARTS LIST NO
A	07397	PL

SHEET 1 OF 2

ESG-1085.8 (1-74)

NOTES: 1. TEXAS INSTRUMENTS
2. CIRCUIT ASSEMBLY CORP

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
			-1							
			1	R				SCHEMATIC DIAGRAM		1
			20			TID-121		DIODE ARRAY U1-20	1	2
			1			CAD-14P01-2	6-1-CD-012	DIP INTERCONNECT CABLE	2	3
			1					VECTORBOARD D-PATTERN 10 1/2" x 4 3/4"		4
			21				72-701074-1	DIP SOCKETS (WIRE WRAP) 14 PIN		5
										6

KEY:
*-VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING
F–FEET
I–INCHES
B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL

CODE IDENT 07397 | SHEET 2 | REV

ESG - 1086.8 (1-72)

PARTS LIST NO **PL** SK 82-3349

NOTES: (UNLESS OTHERWISE SPECIFIED:)

LTR	REVISION DESCRIPTION	DATE	APPROVED

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42

RECORD OF REVISION STATUS OF EACH SHEET

RELEASE APPD BY

LEVEL				
DWG	1	2	3	4
CHK	1	2	3	4
CONT	1	2	3	4

MODEL

NEXT ASSEMBLY

GOVERNMENT CONTRACT NO

PREP [illegible] DATE 5-23-76

CHK

APPD

APPD

GTE SYLVANIA INCORPORATED
ELECTRONIC SYSTEMS GROUP/WESTERN DIVISION
MOUNTAIN VIEW, CA 94042

HOUSING, KEYBOARD - CENTRAL PROCESSOR (BAS)

SIZE	CODE IDENT	PARTS LIST NO
A	07397	PL SK82-3349

SHEET 1 OF 2

ESG-1086.8 (1-74)

NOTES: 1. ZERO MFG CO
1121 CHESTNUT ST
BURBANK CAL
91503

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
			-1							
			1			-101		HOUSING, M/F ZT44-52A	1	1
			4			MF6301-04		NUT PLATE, RT ANGLE (4-40)		2
			8		96906	MS20470AD2-3		RIVET SOLID (.062 DIA X .19 LG)		3

KEY:
* -VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F–FEET
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A/R–AS REQUIRED
R–REFERENCE

PL SK82-3349

CODE IDENT 07397 | SHEET 2 | REV

ESG - 1086.8 (1-72)

NOTES:

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
			-1							
			1			ZT128-176C-6.12		METAL CAN (AL) (8X11X6.12)		1
			1			ZT128-176C-1.00		METAL CAN, ALUMINUM (8 X 11 X 1.00)		2
			A/R			MS 20257-1	(APPROX 4 1/2 FT.)	HINGE, ALUMINUM, 3/8 LEAF		3
			18			MS20470/AD3-4		RIVET, SOLID, UNIVERSAL HD		4
			1			-101		TAMPER SW BRACKET, AL SHEET .04 THK, 5052-H32		5
			1			-103		PANEL LOCK BRACKET, AL SHEET .06 THK, 5052-H32		6
										7

KEY:
*-VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F–FEET
I–INCHES

B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL SK 82-3379-1

CODE IDENT 07397 | SHEET 2 | REV

ESG - 1086.8 (1-72)

NOTES: (UNLESS OTHERWISE SPECIFIED:)

PARTS LIST NO **PL** SK82-3379-1

LTR	REVISION DESCRIPTION	DATE	APPROVED

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42

RECORD OF REVISION STATUS OF EACH SHEET

RELEASE APPD BY

LEVEL				
DWG	1	2	3	4
CHK	1	2	3	4
CONT	1	2	3	4

MODEL CP-1

NEXT ASSEMBLY SK02-3342-1

GOVERNMENT CONTRACT NO

PREP LF DATE 2/11/76

CHK

APPD

APPD

GTE SYLVANIA INCORPORATED

ELECTRONIC SYSTEMS GROUP/WESTERN DIVISION
MOUNTAIN VIEW, CA 94042

BAS
CENTRAL PROCESSOR
HOUSING MODIFICATION

SIZE	CODE IDENT	PARTS LIST NO
A	07397	PL SK82-3379-1

SHEET 1 OF 2

ESG-1085.8 (1-74)

NOTES: (UNLESS OTHERWISE SPECIFIED:)

PARTS LIST NO PL SK02-3400

LTR	REVISION DESCRIPTION	DATE	APPROVED

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42

RECORD OF REVISION STATUS OF EACH SHEET

RELEASE APPD BY

LEVEL
DWG 1 2 3 4
CHK 1 2 3 4
CONT 1 2 3 4

MODEL EC-1

NEXT ASSEMBLY

GOVERNMENT CONTRACT NO

PREP K W Eske DATE 18 FEB 76

CHK

APPD

APPD

GTE SYLVANIA INCORPORATED
ELECTRONIC SYSTEMS GROUP/WESTERN DIVISION
MOUNTAIN VIEW, CA 94042

ENTRANCE CONTROL
ELECTRONICS PKG

SIZE	CODE IDENT	PARTS LIST NO
A	07397	PL SK02-3400

SHEET 1 OF 3

ESG-1085.8 (1-74)

NOTES: 1. PART TO BE LOCATED ON CCA-I/O INTFC

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
			-1							
			1			SK82-3407-1		ENCLOSURE, ENT CONT		1
			1			SK82-3408-1		BASE PLATE, ENT CONT		2
										3
			1					CIRCUIT CD ASSY-MICRO CMPTR		4
			1					CIRCUIT CD ASSY-I/O INTFC		5
										6
			1			152	(EDWARDS)	ELECTRIC STRIKE		7
			2			8632	(C&K)	SWITCH, PUSH BUTTON-MOMEN.		8
			1			8121R	(C&K)	SWITCH	1	9
			3		96906	MS51959-28		SCREW, MACH, FL (6-32X.38 LG)		10
										11
			1			8018-3	(C&K)	CAP, RED		12
			2			7851-2	(C&K)	CAP, BLK		13
										14
			6					SPACER, (4-40 X.75 LG)		15
										16
			1					CONNECTOR (TO KEYBOARD) 17 PIN MIN		17
			1			E63-60H		SWITCH, TAMPER, ENT. CONT		18
										19
										20
										21
										22

KEY:
*-VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F-FEET
I-INCHES

B-BULK
A/R-AS REQUIRED
R-REFERENCE

PL SK02-3400

CODE IDENT 07397 | SHEET 2 | REV

ESG-1086.8 (1-72)

NOTES:

(KEYBOARD SUBASSEMBLY)

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
			-1							
			1			SK82-3393-1		ENCLOSURE, KEYBOARD		23
			1			SK82-3394-1		BASE PLATE K'BD		24
			1			SK82-3392-1		BRACKET, TMP, SW, K'BD		25
										26
										27
			1			940002 (DWG NO)		KEYBOARD, 12 POS		28
										29
			1			252-9951-0971		LAMP, RED, INCAD. (5V)		30
			1			E63-60H		SWITCH TAMPER K'BD		31
										32
								CONNECTOR (K'BD TO ENT CONT)		33
										34
										35
										36
										37

KEY:
*-VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING
F–FEET
I–INCHES
B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL SK02-3400

CODE IDENT 07397 | SHEET 3 | REV

ESG - 1086.8 (1-72)

NOTES: (UNLESS OTHERWISE SPECIFIED:)

PARTS LIST NO **PL**

LTR	REVISION DESCRIPTION	DATE	APPROVED

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42

RECORD OF REVISION STATUS OF EACH SHEET

RELEASE APPD BY

LEVEL
DWG 1 2 3 4
CHK 1 2 3 4
CONT 1 2 3 4

MODEL

NEXT ASSEMBLY

GOVERNMENT CONTRACT NO

PREP DATE
CHK
APPD
APPD

GTE SYLVANIA INCORPORATED
ELECTRONIC SYSTEMS GROUP/WESTERN DIVISION
MOUNTAIN VIEW, CA 94042

ENTRANCE CONTROL
I/O CIRCUITRY

SIZE	CODE IDENT	PARTS LIST NO
A	07397	PL

SHEET 1 OF 4

ESG-1085.8 (1-74)

NOTES:

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
			-1							
			1	R				SCHEMATIC DIAGRAM		1
			1					RESISTOR 270K ±5% 1/4W (R15)		2
			5					RESISTOR 10K ±5% 1/4W (R1,10,11,16,17)		3
			8					RESISTOR 2.7K± 5% 1/4W (R2 – 9)		4
			1					RESISTOR 220K±5% 1/4W (R12)		5
			4					RESISTOR 2.4K±5% 1/4W (R13,18,19,20)		6
			1					RESISTOR 100K±5% 1/4W (R14)		7
			2			8212		I.C. INPUT/OUTPUT PORT (U1,2)		8
			1			CD4034		I.C. INPUT/OUTPUT REGISTAR (U3)		9
			1			CD4050		I.C. HEX BUFFER (U4)		10
			1			DG190		I.C. ANALOG SWITCH (U5)		11

KEY:
*-VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING
F–FEET
I–INCHES
B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL

CODE IDENT 07397 | SHEET 2 | REV

ESG - 1086.8 (1-72)

NOTES: 1. CHERRY ELECTRICAL PROD.
2. C+K COMPONENTS, INC
3. GRAYHILL

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
			-1							
			1			SN5403	15-823192-1	I.C. QUAD 2-INPUT NAND (O.C.) (U6)		12
			1			SN5400	15-823114-1	I.C. QUAD 2-INPUT NAND (U7)		13
			1			8205		I.C. 1 of 8 DECODER (U8)		14
			1			SN5404	15-823114-3	I.C. HEX INVERTER (U9)		15
			3			TID121		DIODE ARRAY IC (U10, 11, 12)		16
			3			TID139N		DIODE ARRAY IC (U13, 14, 15)		17
			1			2N2222		TRANSISTOR NPN Q1		18
			1			IN4148		DIODE (CR1)		19
			2			E63-60H		SWITCH-TAMPER	1	20
			1			8121		SWITCH-ARM	2	21
			2			39-12		SWITCH-PANIC	3	22

KEY:
* -VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F–FEET
I–INCHES

B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL

CODE IDENT 07397 | SHEET 3 | REV

ESG - 1086.8 (1-72)

NOTES: 4. GEORGE RISK IND.
5. DIALIGHT
6. CLARE-PENDAR

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
			-1							
			1			Type 20-24		SWITCH-DOOR SENSE	4	23
			1			252-9951-0971		PILOT LAMP (RED)	5	24
			1			940002		KEYBOARD	6	25
			10				72-701074-1	SOCKET 14 PIN WW DIP		26
			6				72-701074-2	SOCKET 16 PIN WW DIP		27
			3				72-701074-3	SOCKET 24 PIN WW DIP		28

KEY:
*-VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING
F—FEET
I—INCHES
B—BULK
A/R—AS REQUIRED
R—REFERENCE

PL

CODE IDENT 07397 | SHEET 4 | REV

ESG - 1086.8 (1-72)

NOTES:

BAS DATA LINK TRANSMITTER 17 DEC., '75

QUANTITY REQUIRED	KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
		C1			CAPACITOR, CERAMIC, 0.1 μf, 50 V		
		C2			CAP., CER., 0.1 μf, 50 V		
		C3			CAP., CER., 0.1 μf, 50 V		
		C4			CAP., CER., 0.1 μf, 50 V		
		C5			CAP., CER., 0.1 μf, 50 V		
		C6			CAP., MYLAR, 0.1 μf, ±10%, 80 V		✓
		C7			CAP., CER., 0.01 μf, 200 V		
		C8			CAP., CER., 0.01 μf, 200 V		
		C9			CAP., 150 pf ±5%, MICA		✓
					CMR05F151JODL (STORE		

KEY:
* VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING
F–FEET
I–INCHES
B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL

CODE IDENT 07397 | SHEET 1 | REV

ESG - 1086.8 (1-72)

NOTES:

BAS DATA LINK TRANSMITTER 17 DEC., '75

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
					C10			CAP., MICA, 220 pf ± 5 %, CMR05F221JODL (STORES)		✓
					C11			CAP., CER., 0.01 μf		
					C12			CAP, CER, 1000 pf		
					C13			CAP., CER., 0.01 μf		
					C14			CAP., CER., 0.01 μf		
					C15			CAP., TANT., ELECTROLYTIC, 10 μf, 20 V		
					C16			CAP., CER., 0.1 μf., 50 V		
					C17			CAP., MYLAR, 0.018 μf ± 10%, 80 V		
					C18			CAP., MYLAR, 0.022 μf ± 10%, 80 V		
					C19			CAP., MYLAR, 0.047 μf ± 10%, 600 V		
					C20			CAP., CER., 0.1 μf, 50 V		

KEY:
* VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F–FEET
I–INCHES

B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL

CODE IDENT 07397 | SHEET 2 | REV

ESG - 1086.8 (1-72)

NOTES:

BAS DATA LINK TRANSMITTER 13 DEC., 75

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
					C 21			CAP., CER., 0.1 μf, 50 V		
					CR 1			DIODE, 1N4003		
					CR 2			DIODE, 1N4148		
					CR 3			DIODE, 1N4148		
					CR 4			DIODE, 1N4148		
					CR 5			DIODE, 1N4148		
					CR 6			VARACTOR, MOTOROLA MV 2115		
					CR 7			DIODE, 1N4148		
					CR 8			DIODE, 1N4148		
					CR 9			DIODE, 1N4148		

KEY:
* VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F–FEET
I–INCHES

B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL

CODE IDENT 07397	SHEET 3	REV

ESG - 1086.8 (1-72)

NOTES:

BAS DATA LINK TRANSMITTER 18 DEC., '75

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
					L1			INDUCTOR, 220 μH, ±10%,		
								MS 75089-15		
					L2			IND., VAR., 68 μH,		
								CAMBION 7105-45		✓
					L3			IND., 6.8 μH ± 10%		
								MS 75089-11		
					L4			IND., 1.0 mH ± 10%		
								MS 75089-23		
					L5			IND, VAR., 82 μH		
								CAMBION 7105-47		✓
					U1			I.C., RCA CD 4030 AE		
					U2			I.C., CD 4001 AE		
					U3			I.C., CD 4001 AE		
					U4			I.C., CD 4024 AE		

KEY:
* - VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F–FEET
I–INCHES

B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL

CODE IDENT 07397 | SHEET 4 | REV

ESG - 1086.8 (1-72)

NOTES:

BAS DATA LINK TRANSMITTER 12 DEC, '75

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
					AR 1			I.C., RCA CA 3080 A		
					AR 2			I.C., CA 3080 A		
					AR 3			I.C., CA 3080 A		
					R 1			RESISTOR, 120 K ± 5%		
					R 2			RES., 330 K ± 5%		
					R 3			RES., 1.5 MEG., ± 5%		
					R 4			RES., 1.5 MEG., ± 5%		
					R 5			RES., 1.5 MEG., ± 5%		
					R 6			RES., 1.5 MEG., ± 5%		
					R 7			RES., 3.3 MEG., ± 5%		

KEY:
*-VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING
F—FEET
I—INCHES
B—BULK
A/R—AS REQUIRED
R—REFERENCE

PL

CODE IDENT 07397 | SHEET 5 | REV

ESG - 1086.8 (1-72)

NOTES:

BAS DATA LINK TRANSMITTER 18 DEC., '75

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
					R 8			RES., 560 K ± 5%		
					R 9			RES., 270 K ± 5% (SELECTED IN TEST)		
					R 10			RES., 120 K ± 5%		
					R 11			RES., 680 K ± 5%		
					R 12			RES., 680 K ± 5%		
					R 13			RES., 33 K ± 5%		
					R 14			RES., 22 K ± 5%		
					R 15			RES., 22 K ± 5%		
					R 16			RES., 33 K ± 5%		
					R 17			RES., 8200 ± 5%		
					R 18			RES., 8200 ± 5%		

KEY:
* VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F–FEET
I–INCHES

B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL

CODE IDENT 07397 | SHEET 6 | REV

ESG - 1086.8 (1-72)

NOTES:

BAS DATA LINK TRANSMITTER 18 DEC., '75

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
					R 19			RES., 8200 ± 5%		
					R 20			RES., 270 K ± 5%		
					R 21			RES., 470 K ± 5%		
					R 22			RES., 150 ± 5%		
					R 23			RES., 680 ± 5%		
					R 24			RES., 15 K ± 5%		
					R 25			RES., 150 ± 5%		
					R 26			RES., 6800 ± 5%		
					R 27			RES., 10 K ± 5%		
					R 28			RES., 10 K ± 5%		
					R 29			RES., 560 K ± 5%		

KEY:
*-VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F–FEET
I–INCHES

B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL

CODE IDENT 07397 | SHEET 7 | REV

ESG - 1086.8 (1-72)

NOTES:

BAS DATA LINK TRANSMITTER 18 DEC., 75

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
					R 30			RES., 470 K ± 5%		
					R 31			RES., 2200 ± 5%		
					R 32			RES., 33 K ± 5%		
					R 33			RES., 10 ± 5%		
					R 34			RES., 270 ± 5%		
					R 35			RES., 5.6 ± 5%		
					R 36			RES., 390 K ± 5%		
					R 37			RES., 33 K ± 5%		
					R 38			RES., 390 K ± 5%		
					R 39			RES., 53 K ± 5%		
					R 40			RES., 3.3 MEG ± 5%		

KEY:
* VENDOR ITEM · FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F–FEET
I–INCHES

B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL

CODE IDENT 07397 | SHEET 8 | REV

ESG · 1086.8 (1-72)

NOTES:

BAS DATA LINK TRANSMITTER

18 DEC., '75

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
					R 41			RES., 33 K ± 5 %		
					R 42			RES., 390 K ± 5 %		
					R 43			RES., 390 K ± 5 %		
					R 44			RES., 3.3 MEG ± 5 %		
					R45			RES., 390 K ± 5 %		
					R46			RES., 390 K ± 5 %		
					T1			TRANS., CORE: INDIANA GENERAL F624-19 H (SYL. BUILD)		
					T2			TRANS., TRIAD F-133P		

A-62

KEY:
* VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F–FEET
I–INCHES

B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL

CODE IDENT 07397 | SHEET 2 | REV

NOTES: (UNLESS OTHERWISE SPECIFIED:)

PARTS LIST NO PL SK82-3407

LTR	REVISION DESCRIPTION	DATE	APPROVED

A-63

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42

RECORD OF REVISION STATUS OF EACH SHEET

RELEASE APPD BY

LEVEL				
DWG	1	2	3	4
CHK	1	2	3	4
CONT	1	2	3	4

MODEL

NEXT ASSEMBLY

GOVERNMENT CONTRACT NO

PREP F Welter DATE 10 FEB 76

CHK

APPD

APPD

GTE SYLVANIA INCORPORATED

ELECTRONIC SYSTEMS GROUP/WESTERN DIVISION
MOUNTAIN VIEW, CA 94042

ENCLOSURE, ELECTRONICS PKG
ENTRANCE CONTROL
BAS

SIZE	CODE IDENT	PARTS LIST NO
A	07397	PL SK82-3407

SHEET 1 OF 2

ESG-1085.8 (1-74)

NOTES: 1. ZERO MFG Co
1121 CHESTNUT ST
BURBANK, CAL
91503

2. PENN ENGINEERING & MFG CORP
DOYLESTOWN, PENNSYLVANIA
18901

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
			-1							
			1			-101		ENCLOSURE M/F Z56-144A	1	1
			2			-103		FILLER, .063 5052-H32 AL SH		2
			1			-105		FILLER, .063 5052-H32 AL SH		3
			2			-107		BOSS, .50 DIA 5052-H32 AL BAR		4
										5
			3		46384	FHS-440-5		STUD, SELF CLINCH (4-40 x .312 LG)	2	6

KEY:
* -VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F-FEET
I-INCHES

B-BULK
A/R-AS REQUIRED
R-REFERENCE

PL SK82-3407

CODE IDENT 07397 | SHEET 2 | REV

ESG - 1086.8 (1-72)

NOTES: (UNLESS OTHERWISE SPECIFIED:)

PARTS LIST NO PL SK82-3408

LTR	REVISION DESCRIPTION	DATE	APPROVED

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42

RECORD OF REVISION STATUS OF EACH SHEET

RELEASE APPD BY

LEVEL

DWG	1	2	3	4
CHK	1	2	3	4
CONT	1	2	3	4

MODEL

NEXT ASSEMBLY

GOVERNMENT CONTRACT NO

PREP J Weber DATE 11 FEB 76

CHK

APPD

APPD

GTE SYLVANIA INCORPORATED
ELECTRONIC SYSTEMS GROUP/WESTERN DIVISION
MOUNTAIN VIEW, CA 94042

BASE PLATE, ELECTRONICS PKG-
ENTRANCE CONTROL
(BAS)

SIZE	CODE IDENT	PARTS LIST NO
A	07397	PL SK82-3408

SHEET 1 OF 2

ESG-1085.8 (1-74)

CONTINUED

3 OF 5

NOTES: 1. MATERIAL (ALLOY) SUBSTITUTE PERMISSABLE TO FACILITATE FABRICATION

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
			-1							
			1			-101		PLATE, .090 5052-H32 AL SHT	1	1
			1			-103		BOSS-.437 5052-H32 AL PLATE	1	2
			2			-105		BOSS-.25 5052-H32 AL SQ BAR	1	3

KEY:
*-VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F–FEET
I–INCHES

B–BULK
A/R–AS REQUIRED
R–REFERENCE

PL SK 82-3408

CODE IDENT 07397 SHEET 2 REV

ESG - 1086.8 (1-72)

NOTES: (UNLESS OTHERWISE SPECIFIED:)

PARTS LIST NO PL SK 82-3394

LTR	REVISION DESCRIPTION	DATE	APPROVED

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42

RECORD OF REVISION STATUS OF EACH SHEET

RELEASE APPD BY

LEVEL

DWG	1	2	3	4
CHK	1	2	3	4
CONT	1	2	3	4

MODEL BAS

NEXT ASSEMBLY

GOVERNMENT CONTRACT NO

PREP [signature] DATE 3FEB76

CHK

APPD

APPD

GTE SYLVANIA INCORPORATED
ELECTRONIC SYSTEMS GROUP/WESTERN DIVISION
MOUNTAIN VIEW, CA 94042

BASE PLATE, KEYBOARD - ENTRANCE CONTROL

SIZE	CODE IDENT	PARTS LIST NO
A	07397	PL SK 82-3394

SHEET 1 OF 2

ESG-1085.8 (1-74)

Base Plate, Keyboard
Entrance Control

NOTES:

1. VLIER ENGG CORP
2333 VALLEY ST
BURBANK, CALIF
91505

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
			-1							
			1			-101		BASE (.250 THK 5052-H32 ALALY)		1
			2		96906	MS16555-17		PIN, DOWEL (.094 DIA X .312 LG)		2
			2			S-48	(VLIER)	SPRING PLUNGER (6-32X.50LG)	1	3

KEY:
*-VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING
F-FEET
I-INCHES
B-BULK
A/R-AS REQUIRED
R-REFERENCE

PL SK 82-3394

CODE IDENT 07397 | SHEET 2 | REV

ESG - 1086.8 (1-72)

NOTES: (UNLESS OTHERWISE SPECIFIED:)

PARTS LIST NO PL SK82-3382

LTR	REVISION DESCRIPTION	DATE	APPROVED

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42

RECORD OF REVISION STATUS OF EACH SHEET

RELEASE APPD BY

LEVEL				
DWG	1	2	3	4
CHK	1	2	3	4
CONT	1	2	3	4

MODEL ST-1

NEXT ASSEMBLY SK03-3389

GOVERNMENT CONTRACT NO

PREP L.F. DATE 2/16/76

CHK

APPD

APPD

GTE SYLVANIA INCORPORATED

ELECTRONIC SYSTEMS GROUP/WESTERN DIVISION
MOUNTAIN VIEW, CA 94042

BAS
SENSOR TRANSMITTER
HOUSING

SIZE	CODE IDENT	PARTS LIST NO
A	07397	PL SK82-3382

SHEET 1 OF 2

ESG-1085.8 (1-74)

NOTES:

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
			-1							
			1			Z 80-80B		CAN, METAL		1
								5X5" UNTRIMED		
			4			ZSP10-1001-2		RT. ANGLE NUT PLATE		2
								8-32		

KEY:
*-VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING

F—FEET
I—INCHES

B—BULK
A/R—AS REQUIRED
R—REFERENCE

PL 5K82-3382

CODE IDENT 07397 | SHEET 2 | REV

ESG-1086.8 (1-72)

A-71

NOTES: (UNLESS OTHERWISE SPECIFIED:)

PARTS LIST NO PL SK 86-3386

LTR	REVISION DESCRIPTION	DATE	APPROVED

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42

RECORD OF REVISION STATUS OF EACH SHEET

RELEASE APPD BY

LEVEL

DWG	1	2	3	4
CHK	1	2	3	4
CONT	1	2	3	4

MODEL ST-1

NEXT ASSEMBLY SK 03-3389

GOVERNMENT CONTRACT NO

PREP L.F. DATE 2-3-76

CHK

APPD

APPD

GTE SYLVANIA INCORPORATED
ELECTRONIC SYSTEMS GROUP/WESTERN DIVISION
MOUNTAIN VIEW, CA 94042

BAS
SENSOR TRANSMITTER
FLOOR PLATE

SIZE	CODE IDENT	PARTS LIST NO
A	07397	PL SK 86-3386

SHEET 1 OF 2

ESG-1086.8 (1-74)

NOTES: 1.

2. KEYSTONE

QUANTITY REQUIRED			-1	KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
			1			-101	MIL-P-18177	PLATE, .09 THK, EPOXY GLASS RESIN	1	1
								APPROX 5"X5" (TYPE GEE)		
			1			#71		9V BATTERY CLIP	2	2
			4			MS20470/AD3	-4	RIVET, SOLID, UNIV. HD.		3
			1			-103	QQ-A-250/8	BRACKET, .040 THK, 5052-H32		4
								AL SH		
			2			LF0001-1		AC PLUG BRACKET		5
			4					EYLET, BRASS .12DIA		6

KEY:
*-VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING
F—FEET
I—INCHES
B—BULK
A/R—AS REQUIRED
R—REFERENCE

PL SK 86-3386
CODE IDENT 07397 SHEET 2 REV

ESG - 1086.8 (1-72)

NOTES: (UNLESS OTHERWISE SPECIFIED:)

PARTS LIST NO PL

LTR	REVISION DESCRIPTION	DATE	APPROVED

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42

RECORD OF REVISION STATUS OF EACH SHEET

RELEASE APPD BY

LEVEL
DWG 1 2 3 4
CHK 1 2 3 4
CONT 1 2 3 4

MODEL

NEXT ASSEMBLY

GOVERNMENT CONTRACT NO

PREP DATE

CHK

APPD

APPD

GTE SYLVANIA INCORPORATED
ELECTRONIC SYSTEMS GROUP/WESTERN DIVISION
MOUNTAIN VIEW, CA 94042

EXTERNAL INTERFACE

SIZE	CODE IDENT	PARTS LIST NO
A	07397	PL

SHEET 1 OF 2

ESG-1085.8 (1-74)

A-73

NOTES: 1. VENTEL CORP.
2. AMP
3. AUGAT

QUANTITY REQUIRED				KEY	CODE IDENT	PART OR IDENTIFYING NO.	GTE SYLVANIA PART NO.	NOMENCLATURE OR DESCRIPTION	NOTE	ITEM NO.
			-1							
			1	R				SCHEMATIC DIAGRAM		1
										2
			1			100-1		MICRO MODEM	1	3
			2					RESISTOR 10 ±5% 1/4W (R1, 2)		4
			1					RESISTOR 560 ±5% 1/4W		5
			2					CAPACITOR 100 μF 20VDC		6
			1			HDP-20-205203-1		CONNECTOR	2	7
			1			HDP-20-205205-1		CONNECTOR	2	8
			3			325-AG1F		CONTACT STRIP	3	9
			1					VECTORBOARD P-PATTERN 3 1/4" × 7"		10
							RJ26CX104	POTENTIOMETER 10-TURN 100K (R3)		11

KEY:
*-VENDOR ITEM - FOR PROCUREMENT OR PART NUMBER SEE SPECIFICATION CONTROL OR SOURCE CONTROL DRAWING
F-FEET
I-INCHES
B-BULK
A/R-AS REQUIRED
R-REFERENCE

PL

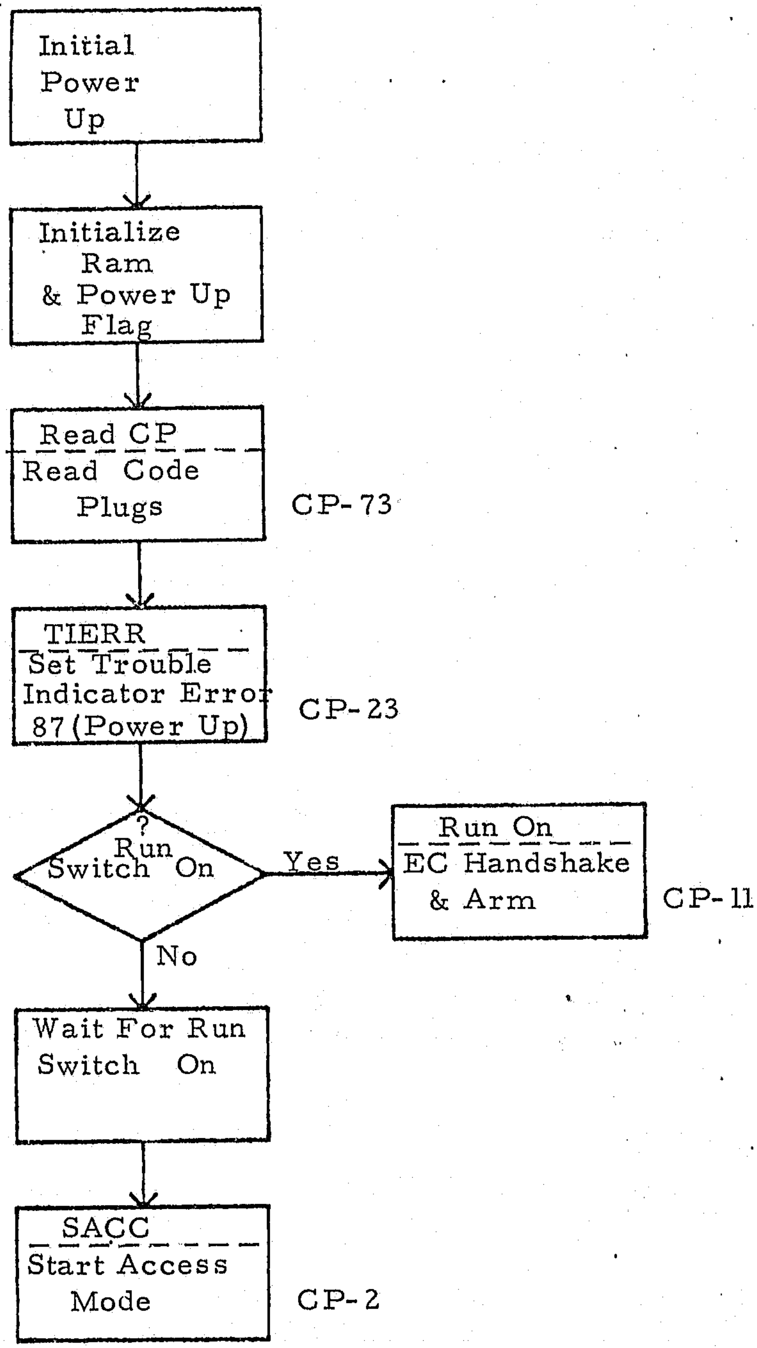
CODE IDENT 07397 | SHEET 2 | REV

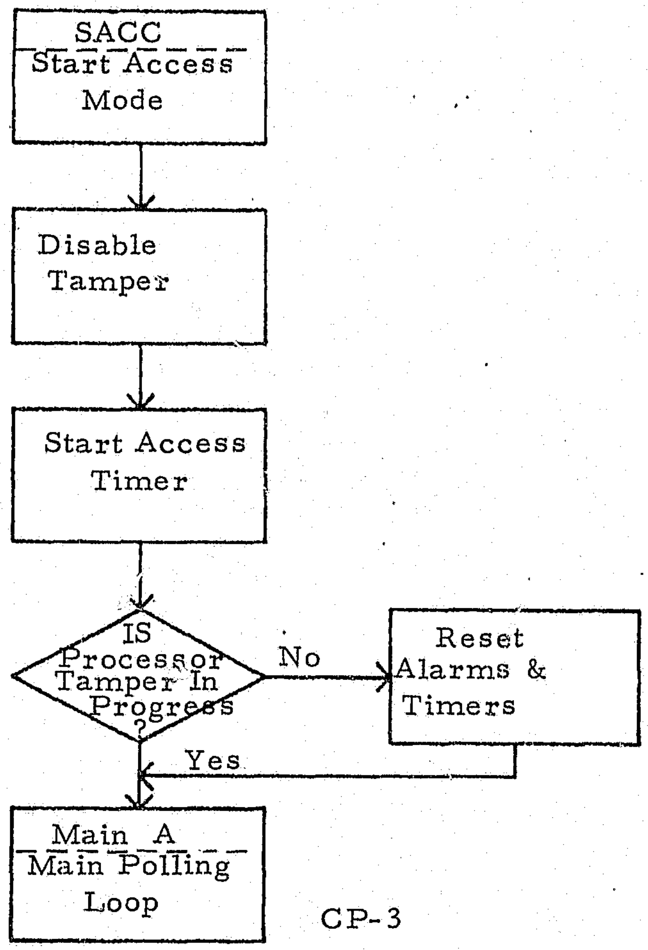
ESG - 1086.8 (1-72)

Appendix B

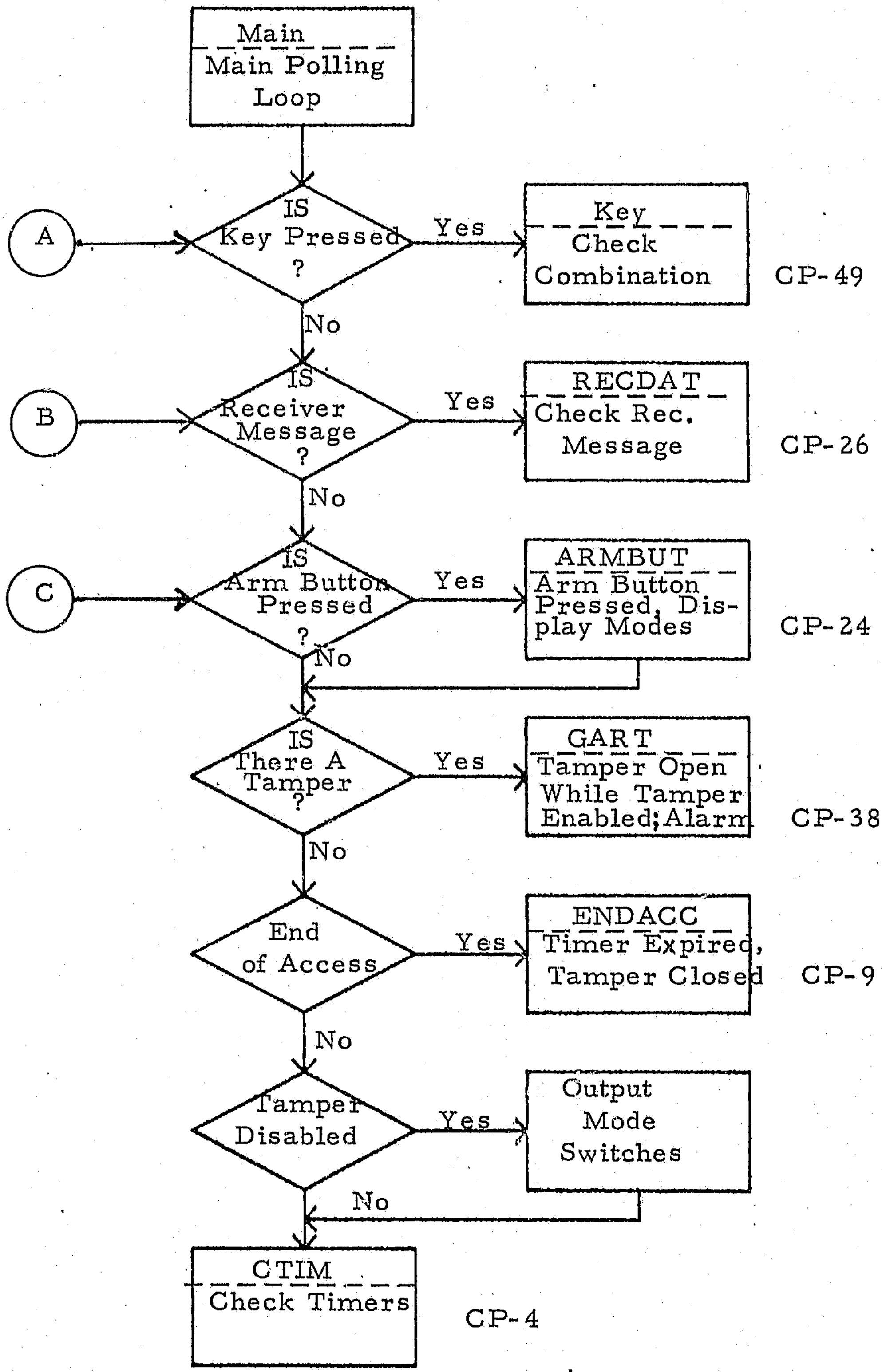
BAS SOFTWARE FLOW DIAGRAMS

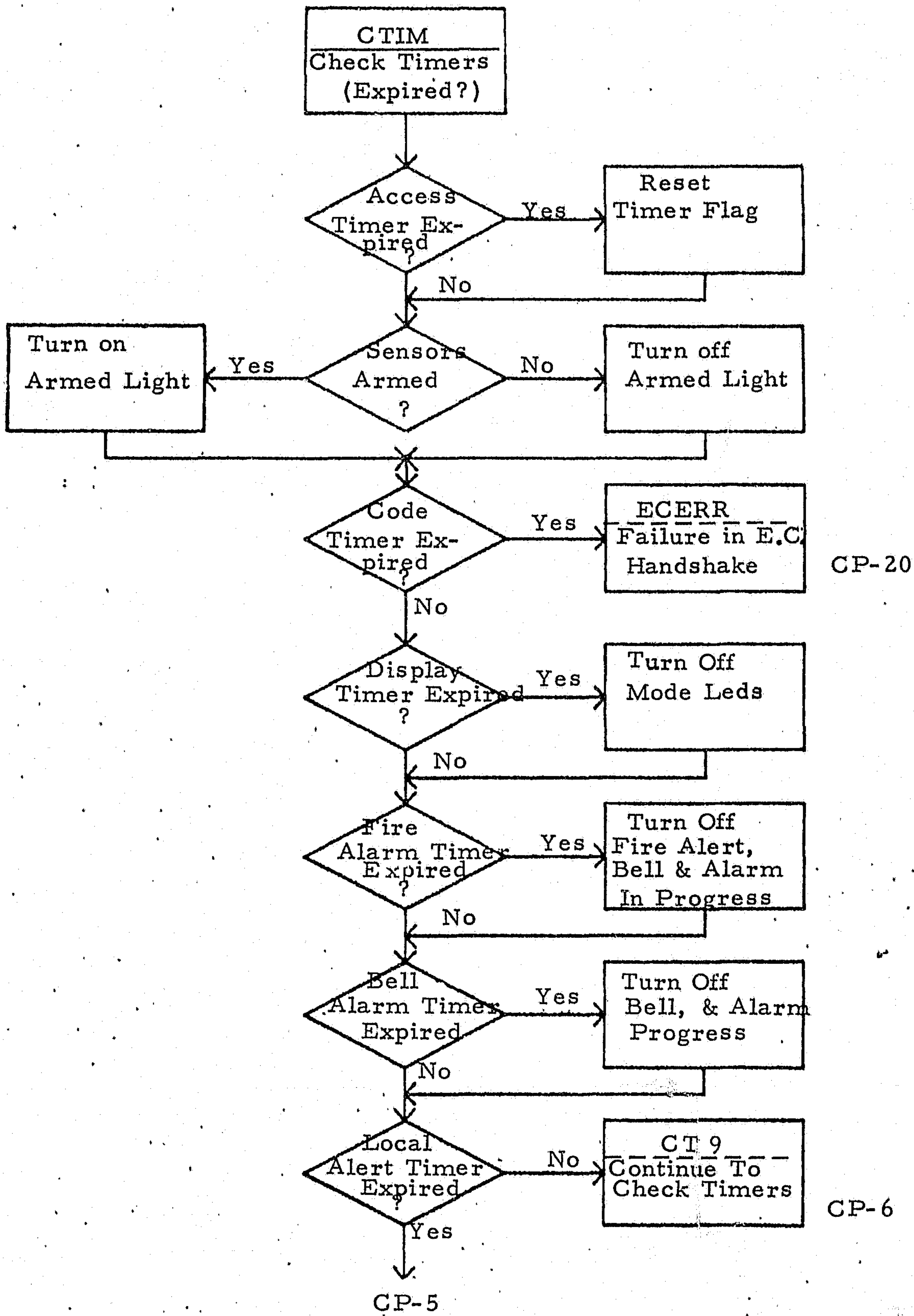
The following pages represent the BAS software flow diagrams illustrating the major program loop with all the subroutines for the central processor, the entrance control and the central station. Pages are numbered consecutively with a prefix of either CP, EC, or CS. These are the routines for the central processor, the entrance control, and the central station.


Initial Power Up
Initialize Ram & Power Up Flag
Read CP
Read Code Plugs
CP-73
TIERR
Set Trouble Indicator Error 87 (Power Up)
CP-23
Run Switch On ?
Yes
No
Run On
EC Handshake & Arm
CP-11
Wait For Run Switch On
SACC
Start Access Mode
CP-2

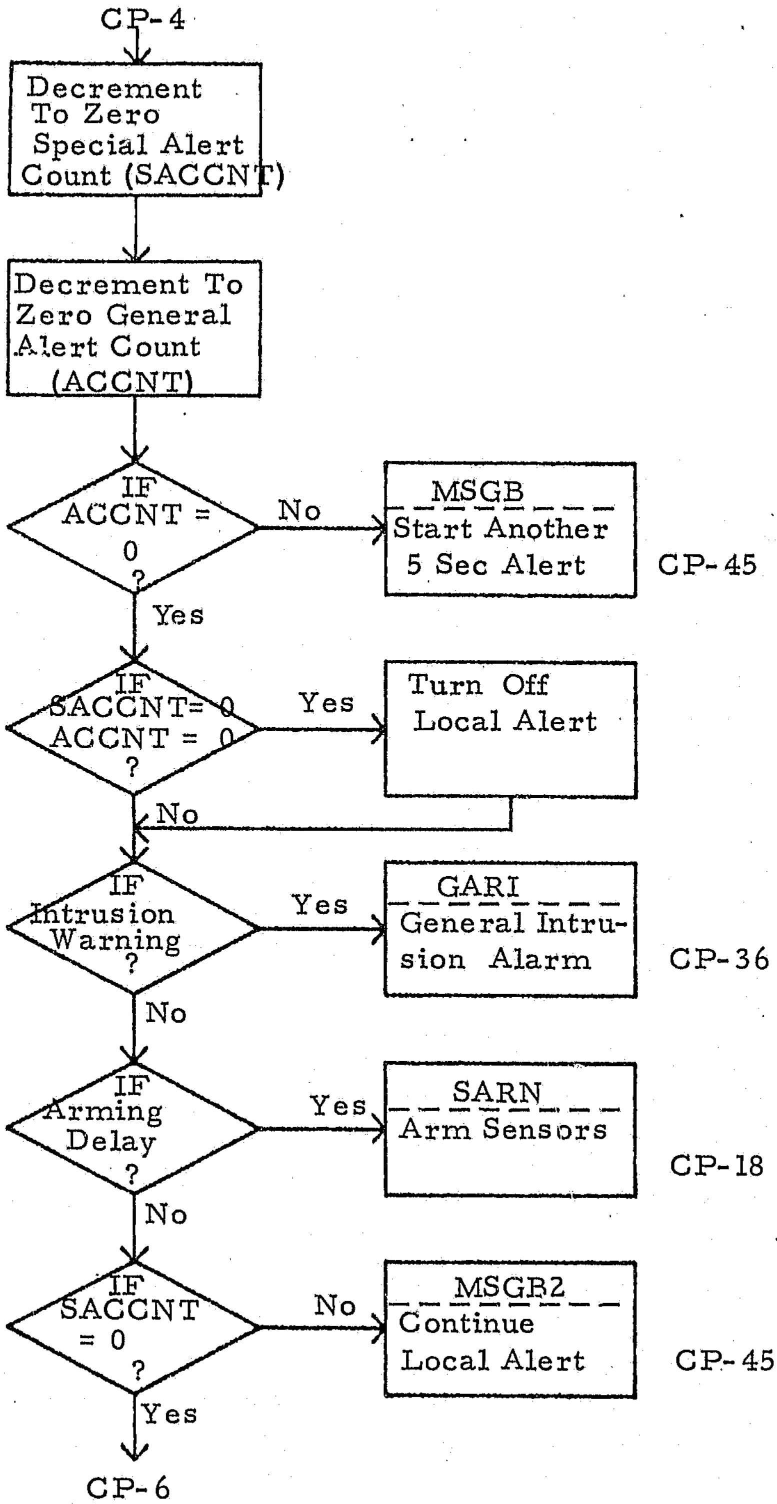

SACC
Start Access Mode
Disable Tamper
Start Access Timer
IS Processor Tamper In Progress ?
No
Reset Alarms & Timers
Yes
Main A
Main Polling Loop

CP-3

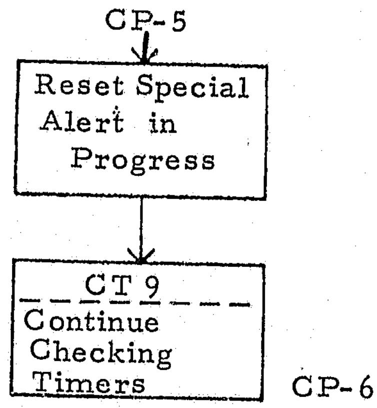

Main
Main Polling Loop
A
IS Key Pressed ?
Yes
Key
Check Combination
CP-49
No
B
IS Receiver Message ?
Yes
RECDAT
Check Rec. Message
CP-26
No
C
IS Arm Button Pressed ?
Yes
ARMBUT
Arm Button Pressed, Display Modes
CP-24
No
IS There A Tamper ?
Yes
GART
Tamper Open While Tamper Enabled; Alarm
CP-38
No
End of Access
Yes
ENDACC
Timer Expired, Tamper Closed
CP-9
No
Tamper Disabled
Yes
Output Mode Switches
No
CTIM
Check Timers
CP-4

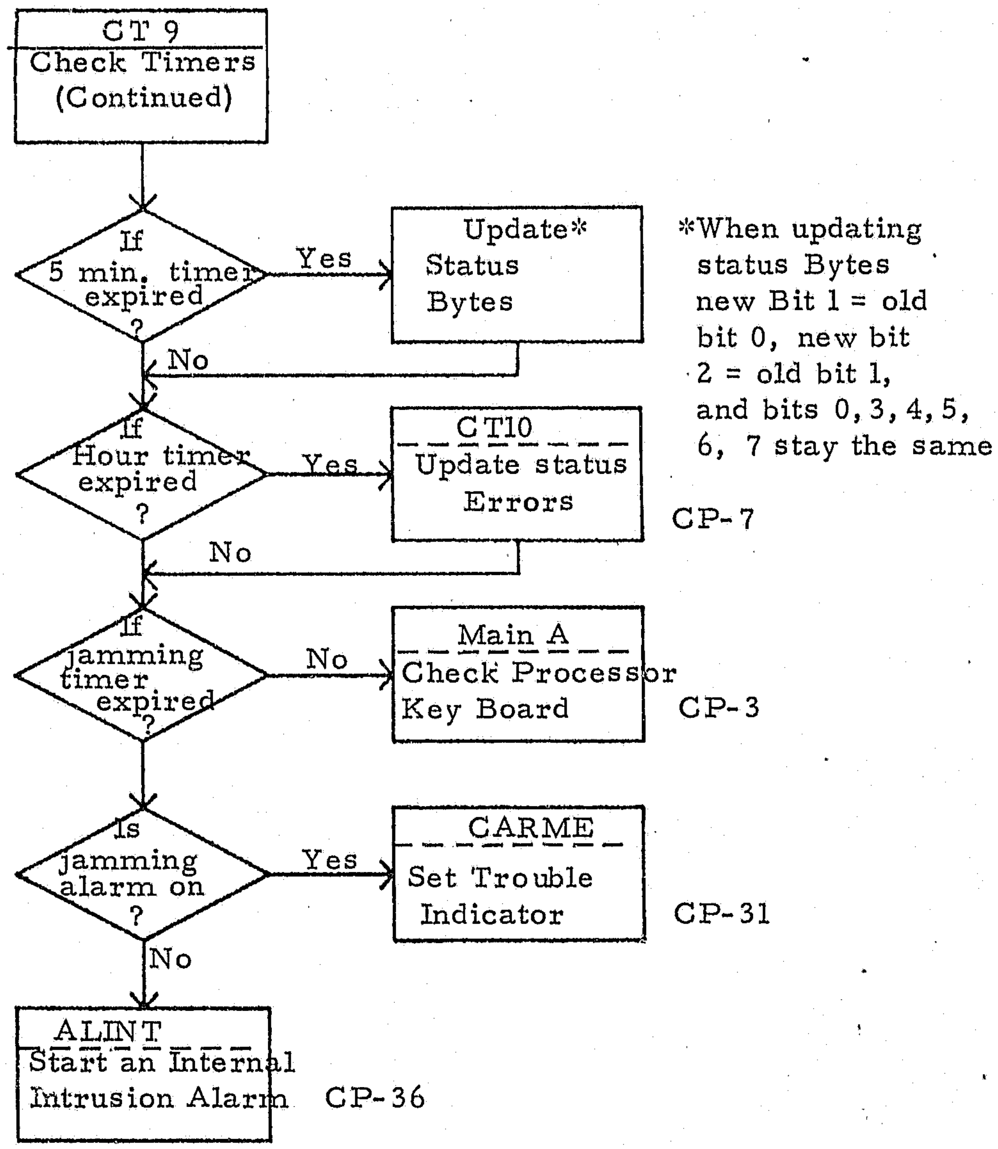


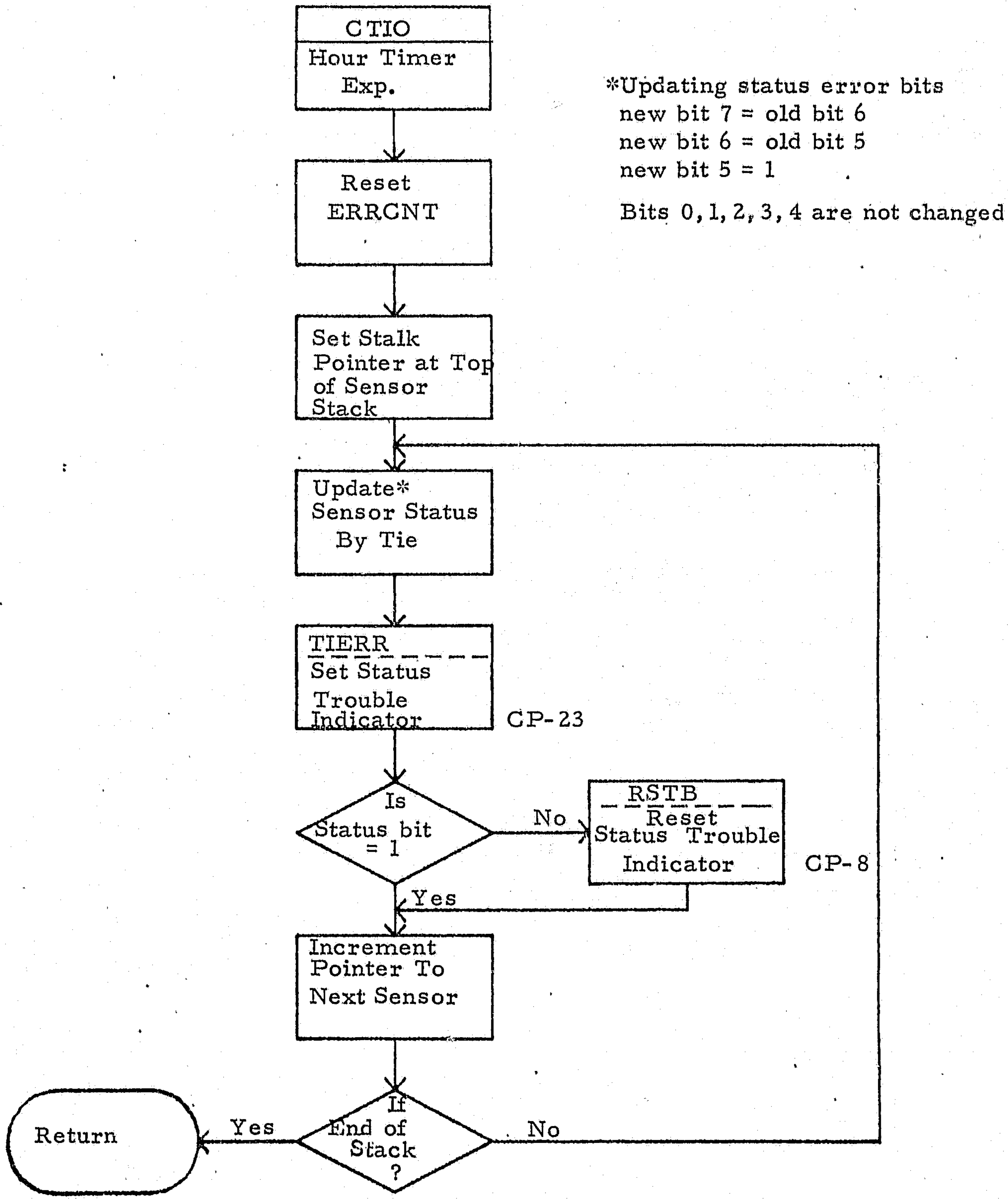
CTIM
Check Timers (Expired?)
Access Timer Expired ?
Yes
Reset Timer Flag
No
Turn on Armed Light
Yes
Sensors Armed ?
No
Turn off Armed Light
Code Timer Expired ?
Yes
ECERR
Failure in E.C. Handshake
CP-20
No
Display Timer Expired ?
Yes
Turn Off Mode Leds
No
Fire Alarm Timer Expired ?
Yes
Turn Off Fire Alert, Bell & Alarm In Progress
No
Bell Alarm Timer Expired
Yes
Turn Off Bell, & Alarm Progress
No
Local Alert Timer Expired ?
No
CT 9
Continue To Check Timers
CP-6
Yes
CP-5

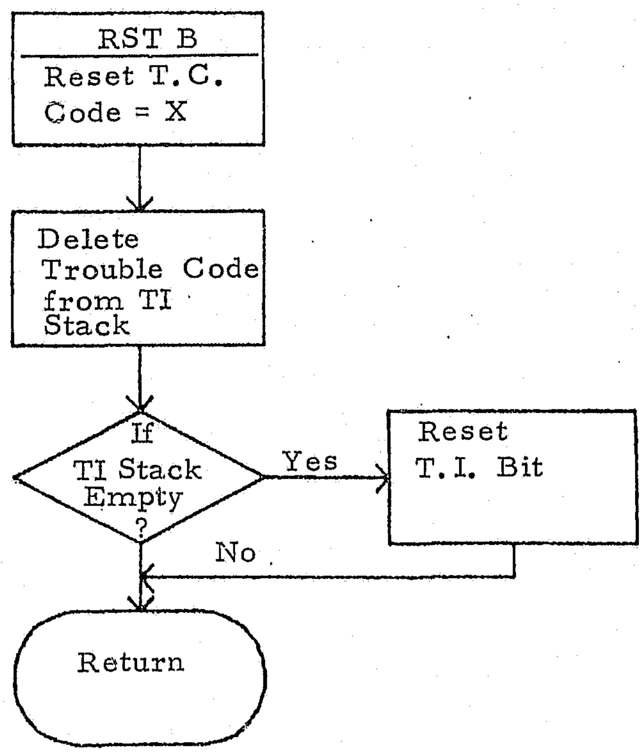

CP-4
Decrement To Zero Special Alert Count (SACCNT)
Decrement To Zero General Alert Count (ACCNT)
IF ACCNT = 0 ?
No
MSGB
Start Another 5 Sec Alert
CP-45
Yes
IF SACCNT= 0 ACCNT = 0 ?
Yes
Turn Off Local Alert
No
IF Intrusion Warning ?
Yes
GARI
General Intrusion Alarm
CP-36
No
IF Arming Delay ?
Yes
SARN
Arm Sensors
CP-18
No
IF SACCNT = 0 ?
No
MSGB2
Continue Local Alert
CP-45
Yes
CP-6

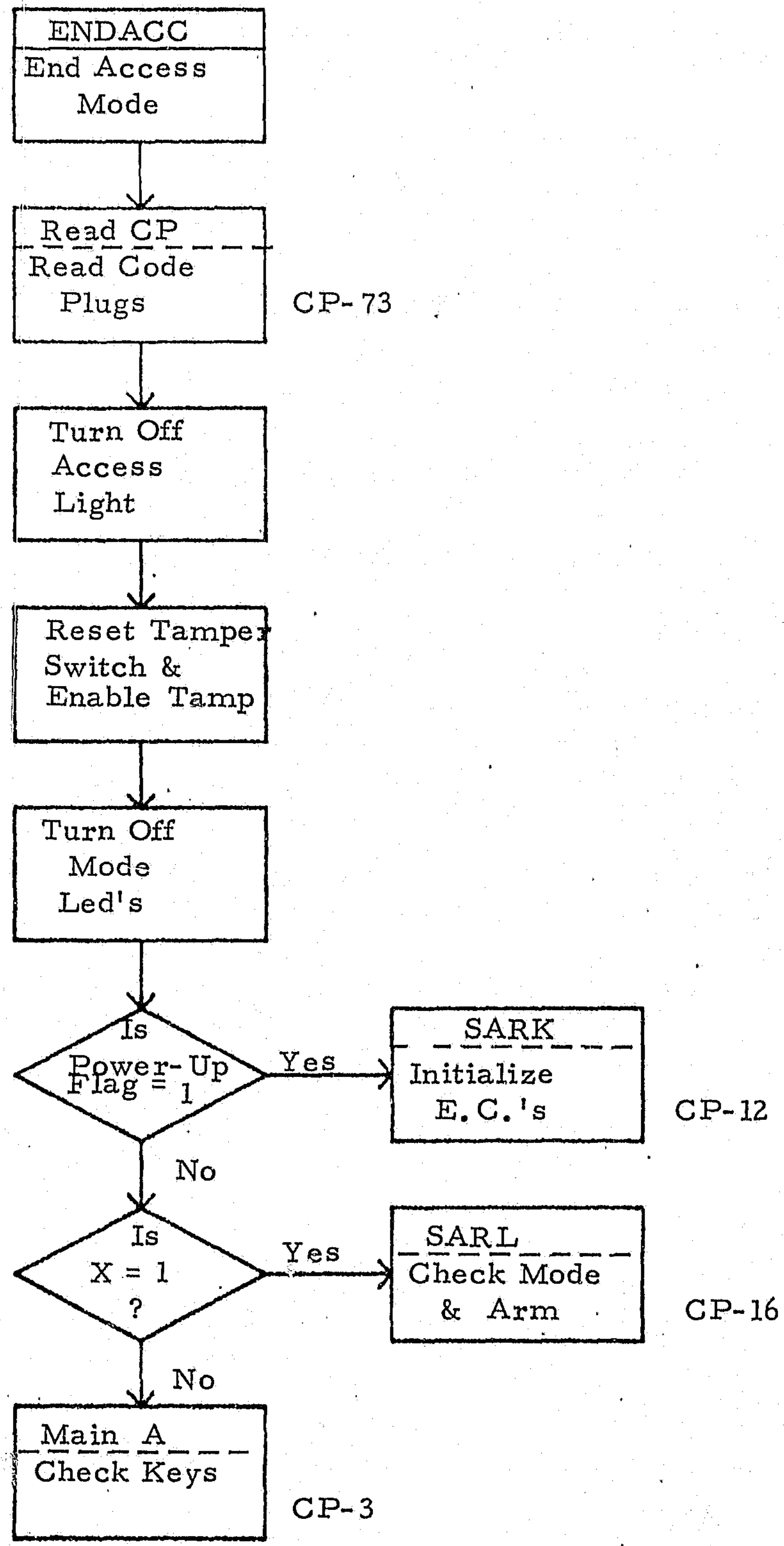
CP-5


CP-5
Reset Special Alert in Progress
CT 9
Continue Checking Timers
CP-6

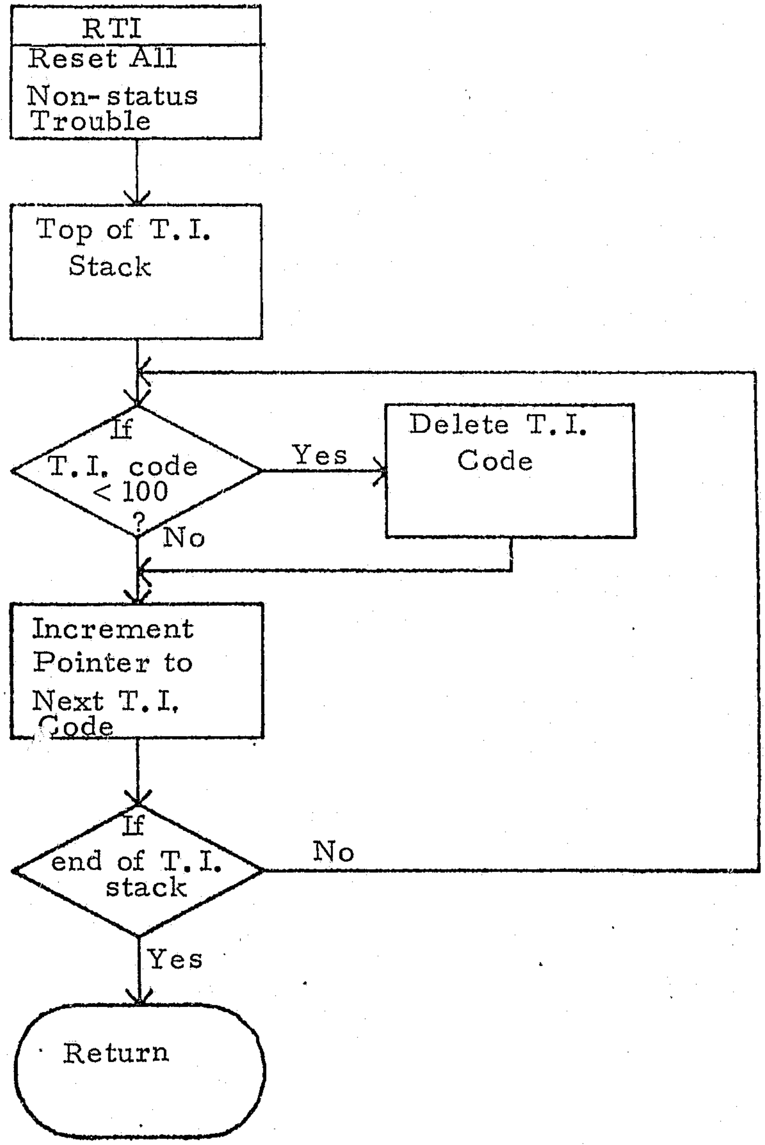

CT 9
Check Timers
(Continued)
If
5 min. timer
expired
?
Yes
Update*
Status
Bytes
*When updating status Bytes new Bit 1 = old bit 0, new bit 2 = old bit 1, and bits 0, 3, 4, 5, 6, 7 stay the same
No
If
Hour timer
expired
?
Yes
CT10
Update status
Errors
CP-7
No
If
jamming
timer
expired
?
No
Main A
Check Processor
Key Board
CP-3
Is
jamming
alarm on
?
Yes
CARME
Set Trouble
Indicator
CP-31
No
ALINT
Start an Internal
Intrusion Alarm
CP-36

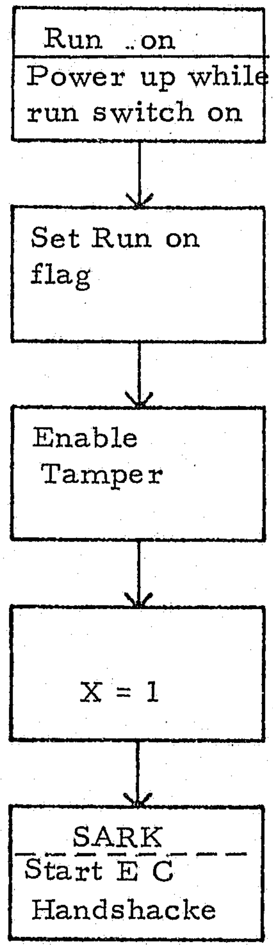

CTIO
Hour Timer Exp.
*Updating status error bits
new bit 7 = old bit 6
new bit 6 = old bit 5
new bit 5 = 1
Bits 0, 1, 2, 3, 4 are not changed
Reset ERRCNT
Set Stalk Pointer at Top of Sensor Stack
Update* Sensor Status By Tie
TIERR
Set Status Trouble Indicator
CP-23
Is Status bit = 1
No
RSTB
Reset Status Trouble Indicator
CP-8
Yes
Increment Pointer To Next Sensor
Return
Yes
If End of Stack ?
No


RST B
Reset T.C.
Code = X
Delete
Trouble Code
from TI
Stack
If
TI Stack
Empty
?
Yes
Reset
T.I. Bit
No
Return



ENDACC
End Access Mode
Read CP
Read Code Plugs
CP-73
Turn Off Access Light
Reset Tamper Switch & Enable Tamp
Turn Off Mode Led's
Is Power-Up Flag = 1
Yes
SARK
Initialize E.C.'s
CP-12
No
Is X = 1 ?
Yes
SARL
Check Mode & Arm
CP-16
No
Main A
Check Keys
CP-3

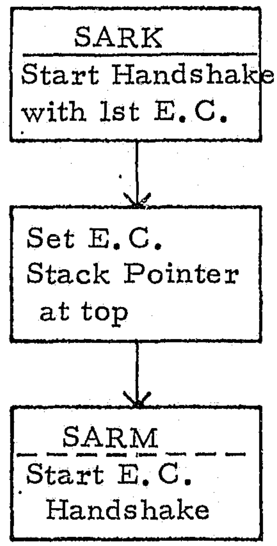

RTI
Reset All
Non-status
Trouble
Top of T.I.
Stack
If
T.I. code
< 100
?
Yes
Delete T.I.
Code
No
Increment
Pointer to
Next T.I.
Code
If
end of T.I.
stack
No
Yes
Return



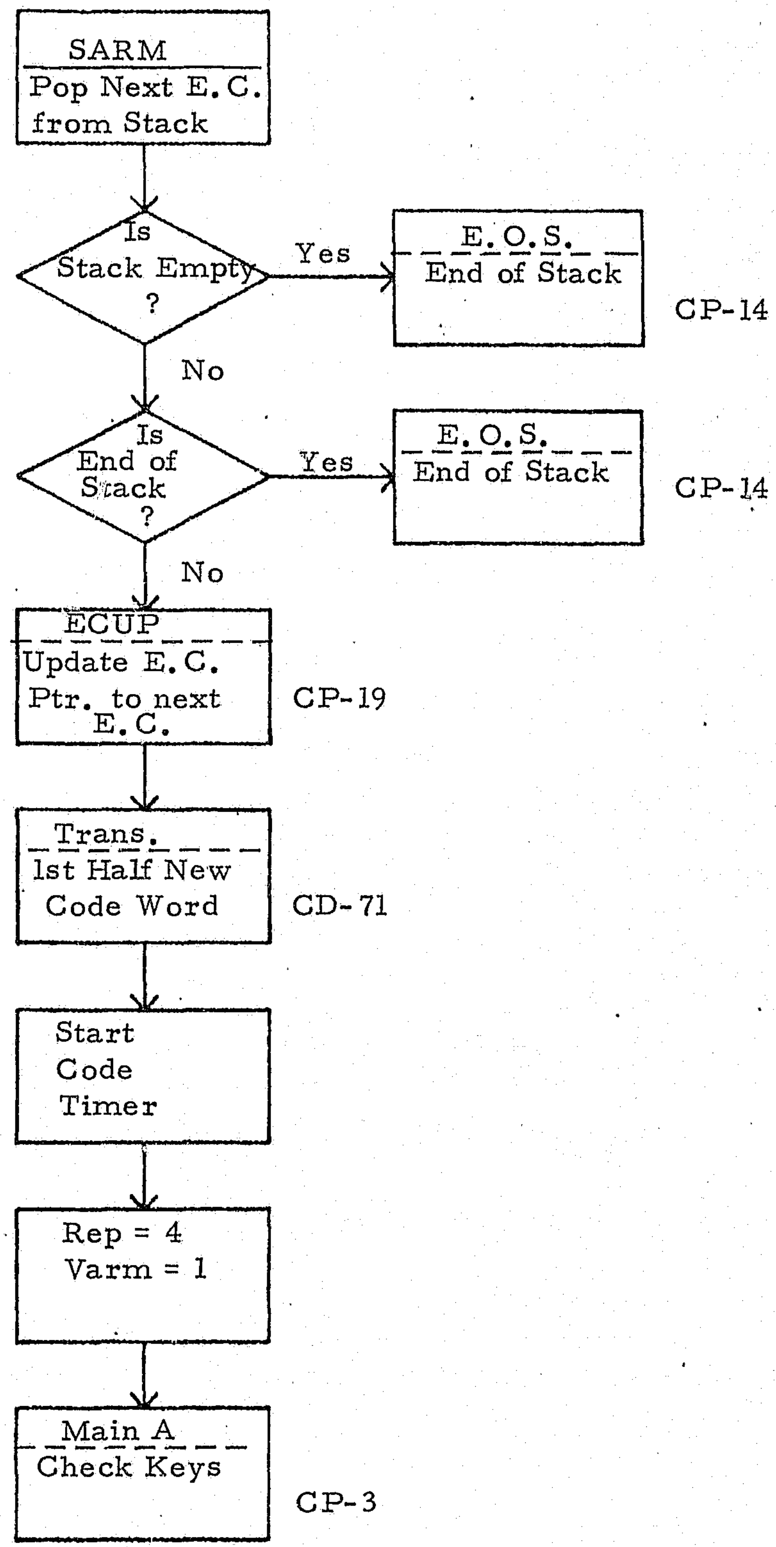
CP-12

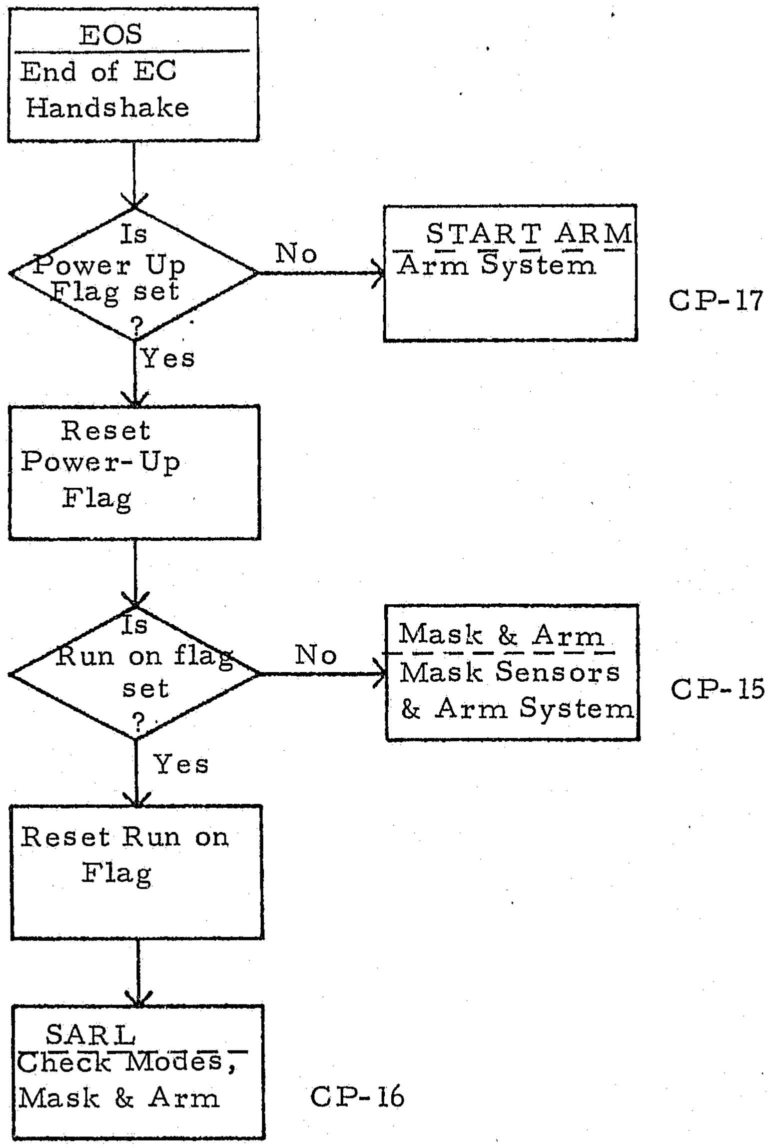
NOTE: X=1; Handshake with Arming

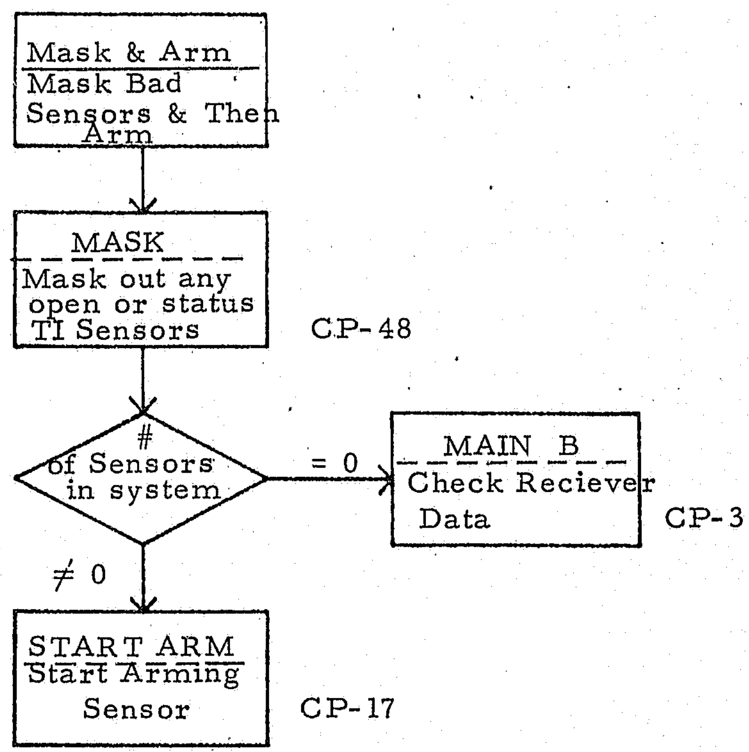
X=0; Handshake without Arming

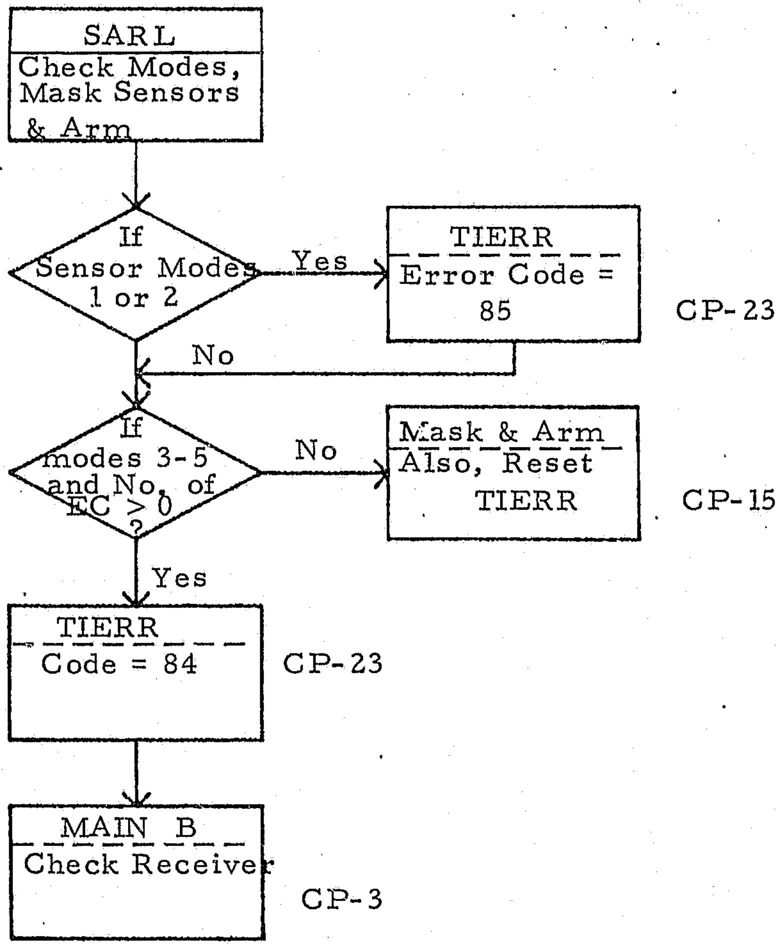

SARK
Start Handshake
with 1st E.C.
Set E.C.
Stack Pointer
at top
SARM
Start E.C.
Handshake

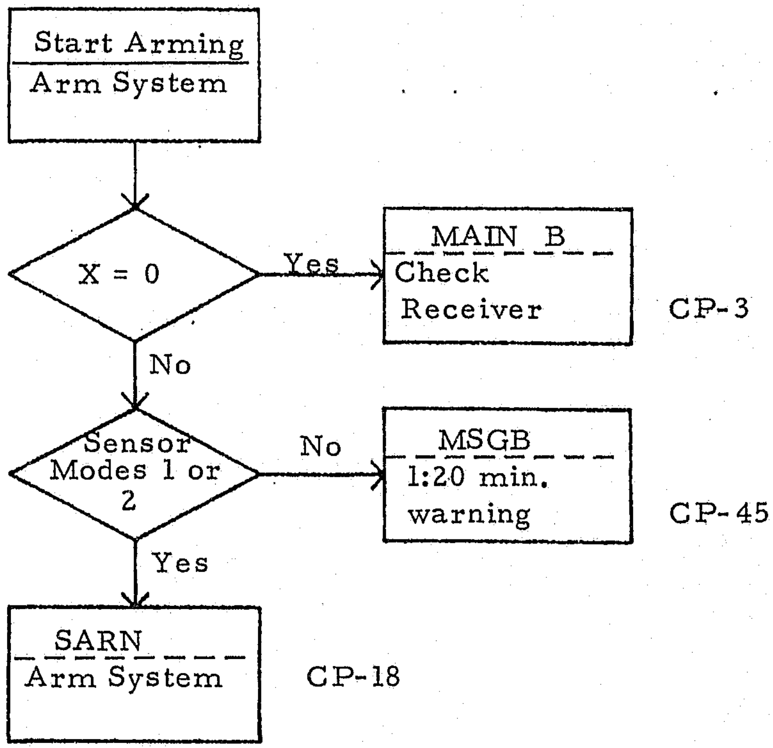
CP-13

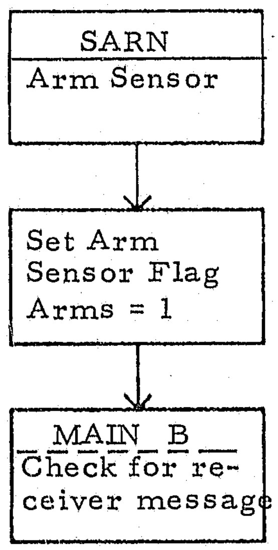

SARM
Pop Next E. C. from Stack
Is Stack Empty ?
Yes
No
E. O. S.
End of Stack
CP-14
Is End of Stack ?
Yes
No
E. O. S.
End of Stack
CP-14
ECUP
Update E. C. Ptr. to next E. C.
CP-19
Trans.
1st Half New Code Word
CD-71
Start Code Timer
Rep = 4
Varm = 1
Main A
Check Keys
CP-3


EOS
End of EC Handshake
Is Power Up Flag set ?
No
START ARM
Arm System
CP-17
Yes
Reset Power-Up Flag
Is Run on flag set ?
No
Mask & Arm
Mask Sensors & Arm System
CP-15
Yes
Reset Run on Flag
SARL
Check Modes, Mask & Arm
CP-16

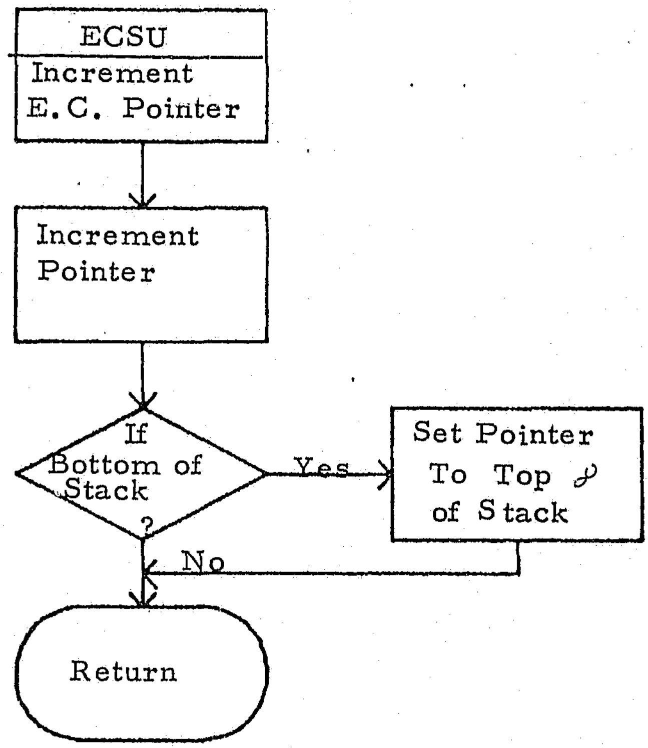

Mask & Arm
Mask Bad Sensors & Then Arm
MASK
Mask out any open or status TI Sensors
CP-48
# of Sensors in system
= 0
MAIN B
Check Reciever Data
CP-3
≠ 0
START ARM
Start Arming Sensor
CP-17

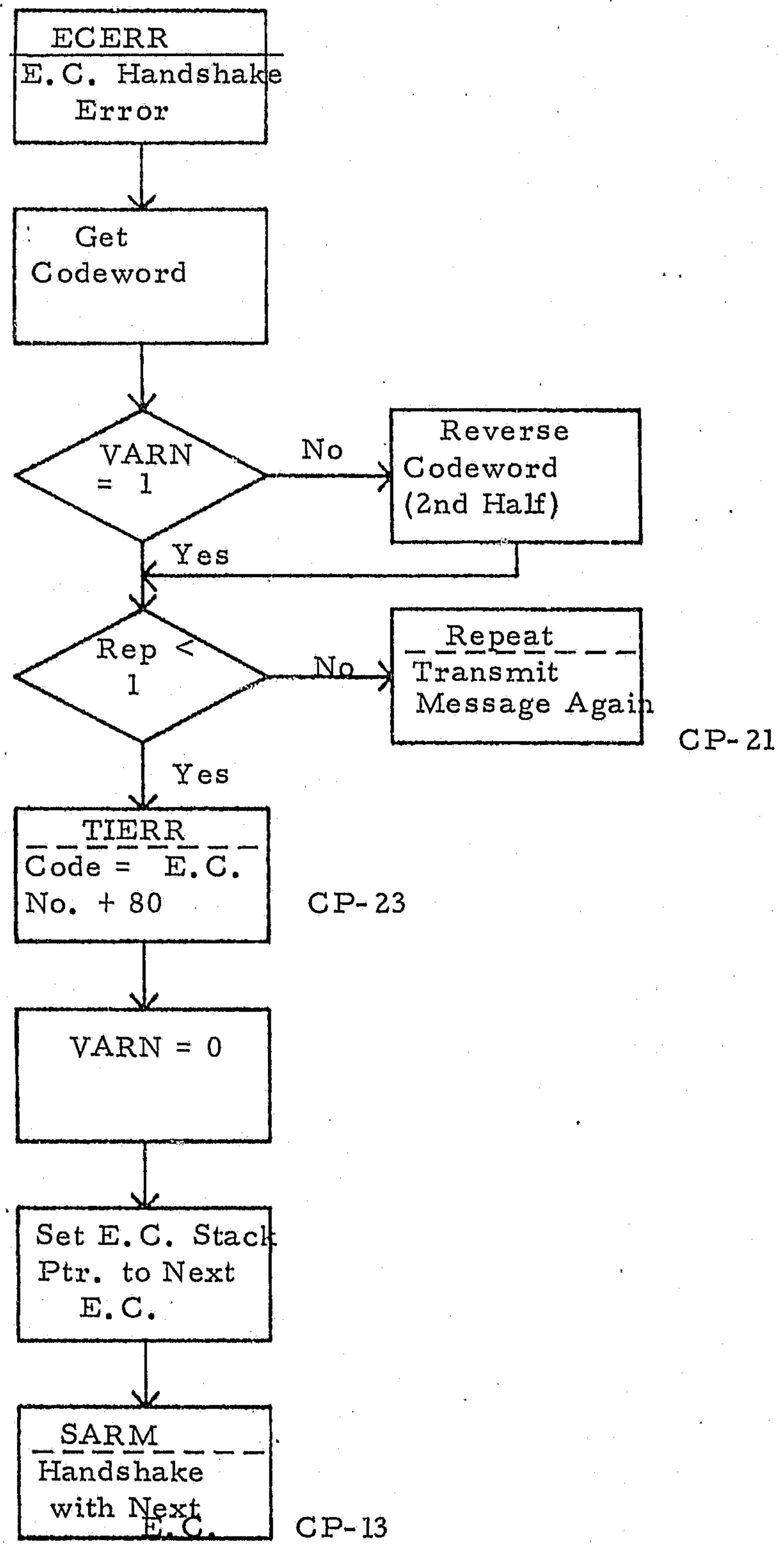

SARL
Check Modes, Mask Sensors & Arm
If Sensor Modes 1 or 2
Yes
TIERR
Error Code = 85
CP-23
No
If modes 3-5 and No. of EC > 0 ?
No
Mask & Arm
Also, Reset TIERR
CP-15
Yes
TIERR
Code = 84
CP-23
MAIN B
Check Receiver
CP-3

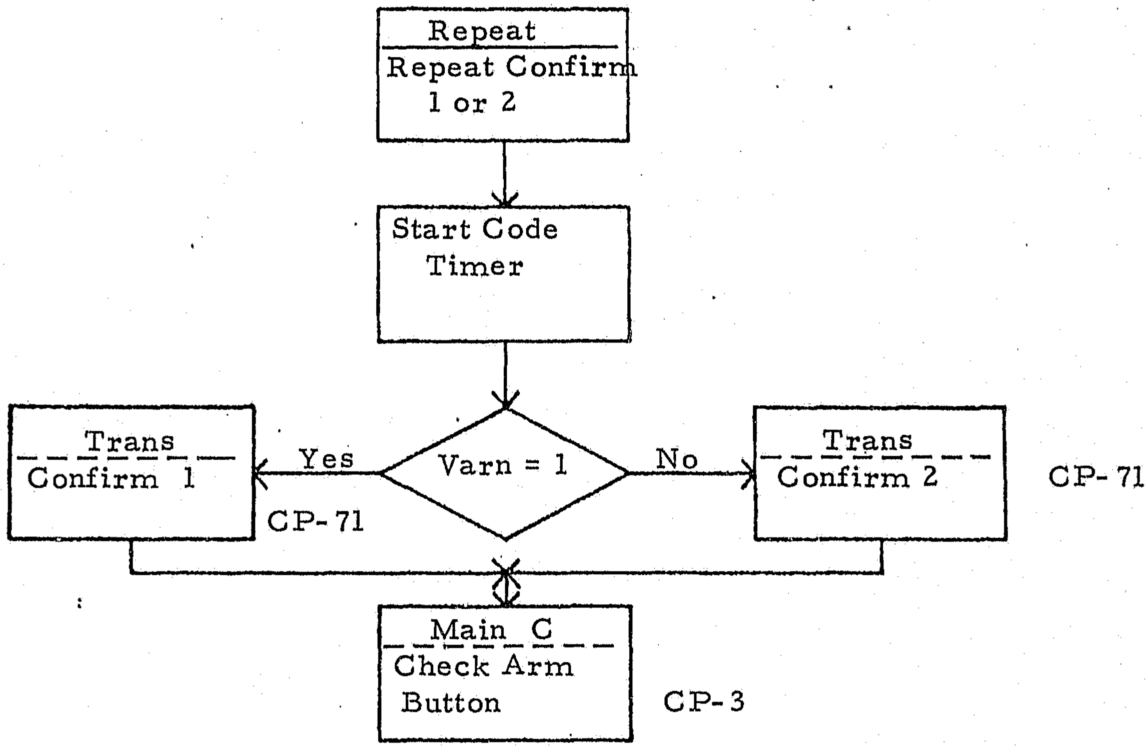

Start Arming
Arm System
X = 0
Yes
MAIN B
Check Receiver
CP-3
No
Sensor Modes 1 or 2
No
MSGB
1:20 min. warning
CP-45
Yes
SARN
Arm System
CP-18

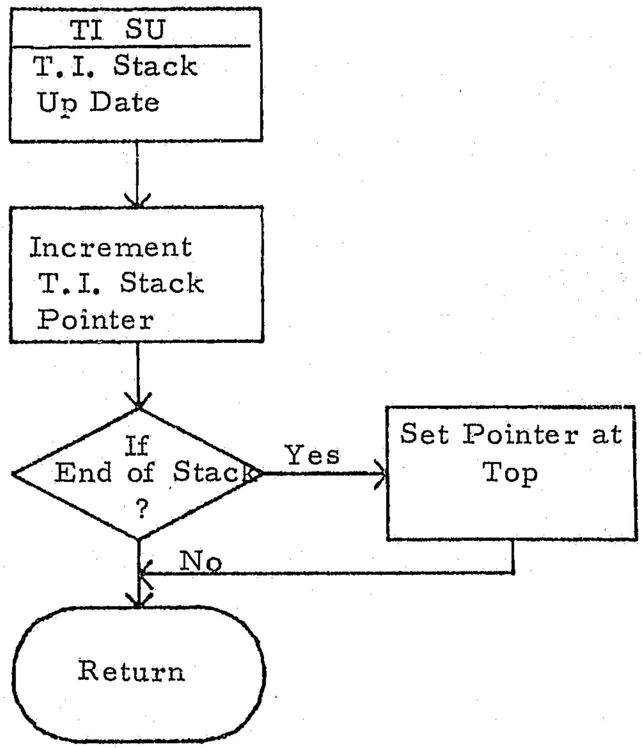

SARN
Arm Sensor
Set Arm
Sensor Flag
Arms = 1
MAIN B
Check for re-
ceiver message

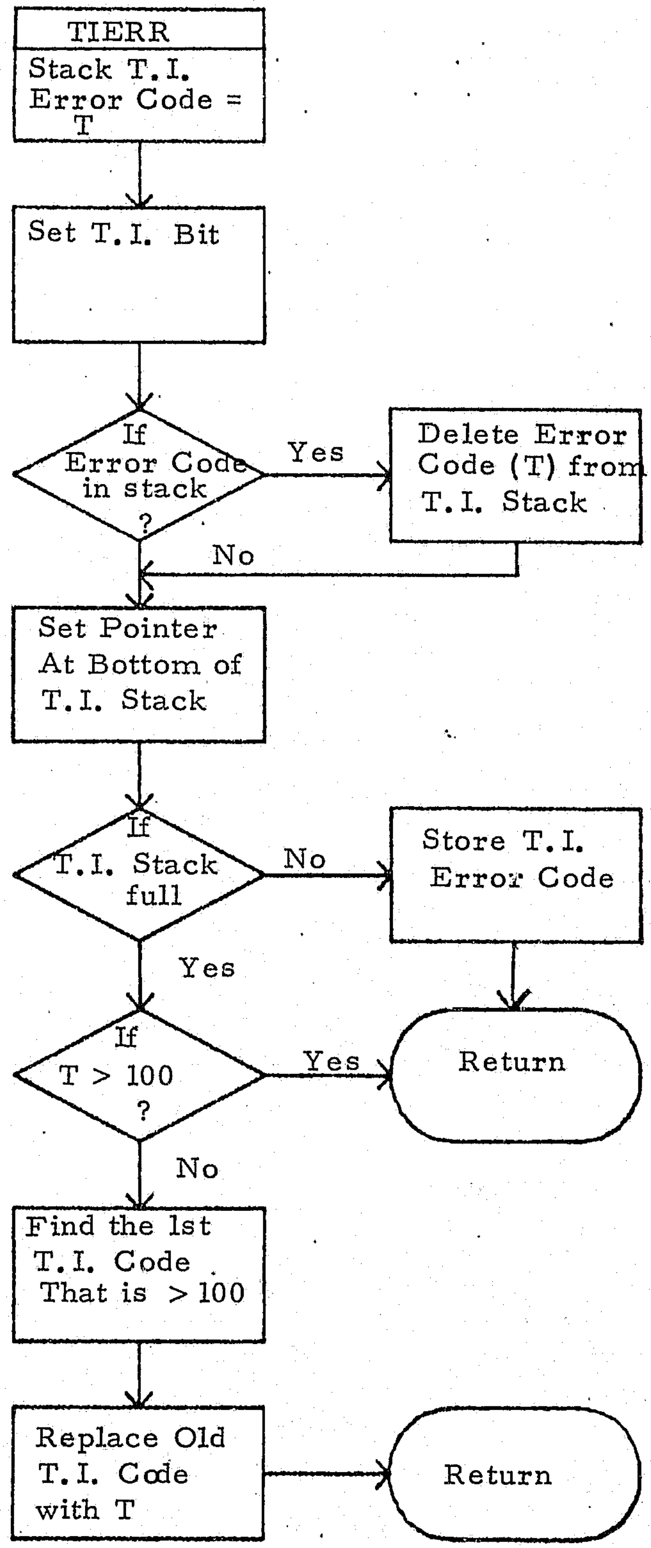
CP-3

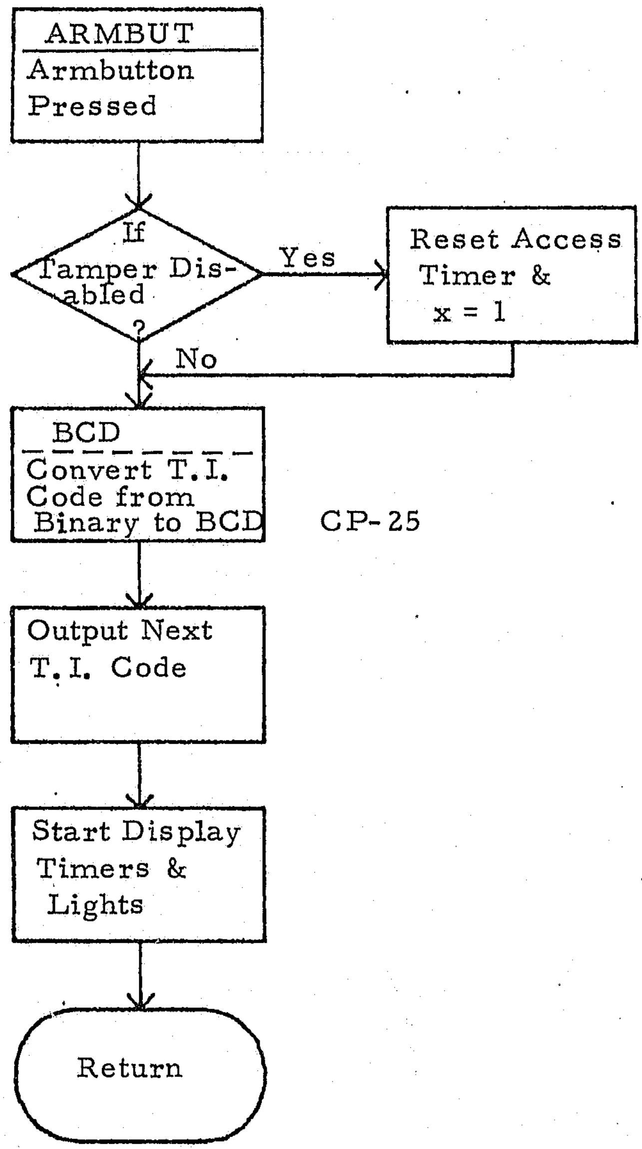

ECSU
Increment
E.C. Pointer
Increment
Pointer
If
Bottom of
Stack
?
Yes
Set Pointer
To Top of
of Stack
No
Return

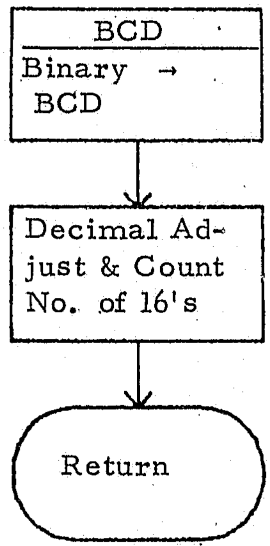

ECERR
E.C. Handshake Error
Get Codeword
VARN = 1
No
Reverse Codeword (2nd Half)
Yes
Rep < 1
No
Repeat
Transmit Message Again
CP-21
Yes
TIERR
Code = E.C. No. + 80
CP-23
VARN = 0
Set E.C. Stack Ptr. to Next E.C.
SARM
Handshake with Next E.C.
CP-13

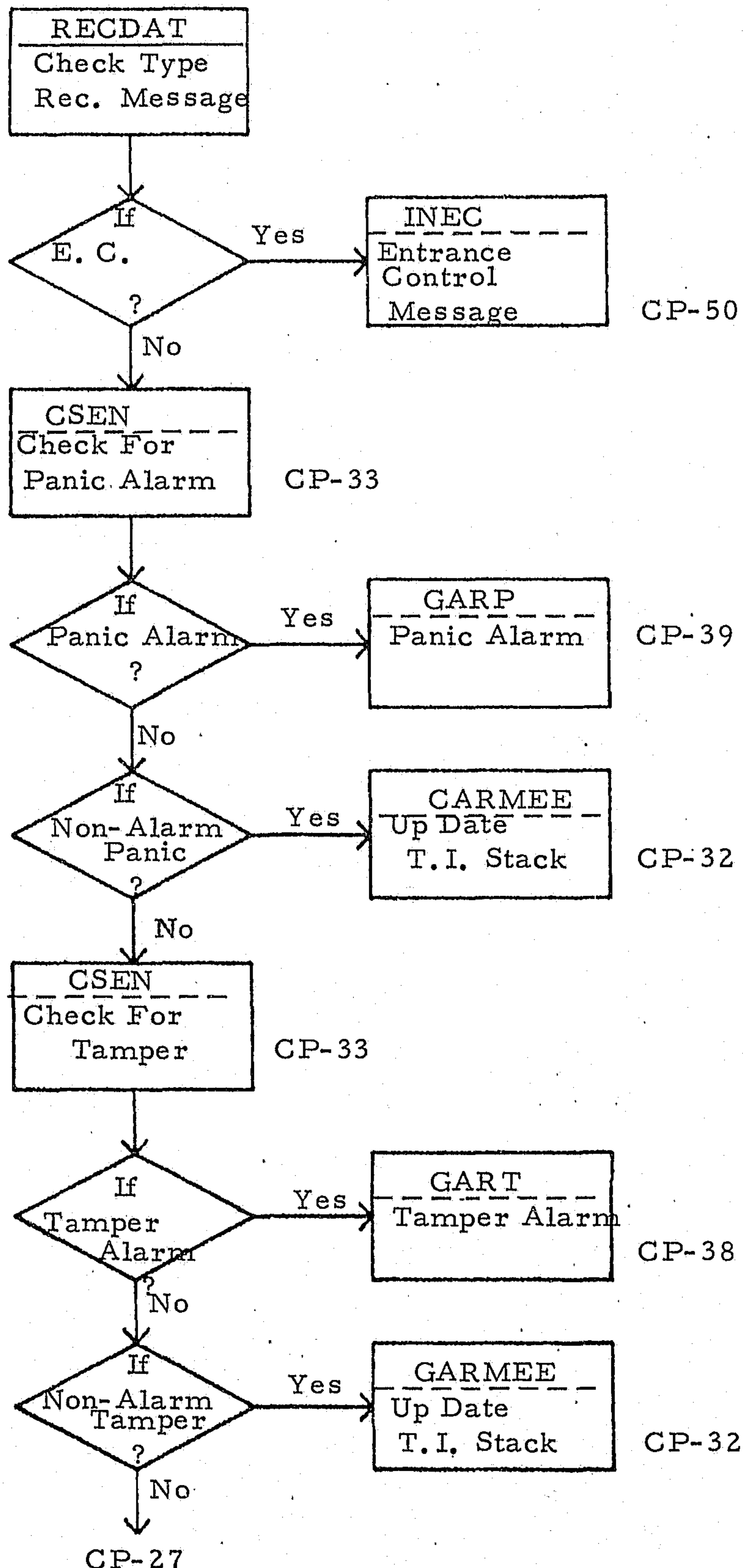

Repeat
Repeat Confirm
1 or 2
Start Code
Timer
Trans
Confirm 1
Yes
Varn = 1
No
Trans
Confirm 2
CP- 71
CP- 71
Main C
Check Arm
Button
CP- 3


TI SU
T.I. Stack
Up Date
Increment
T.I. Stack
Pointer
If
End of Stack
?
Yes
Set Pointer at
Top
No
Return

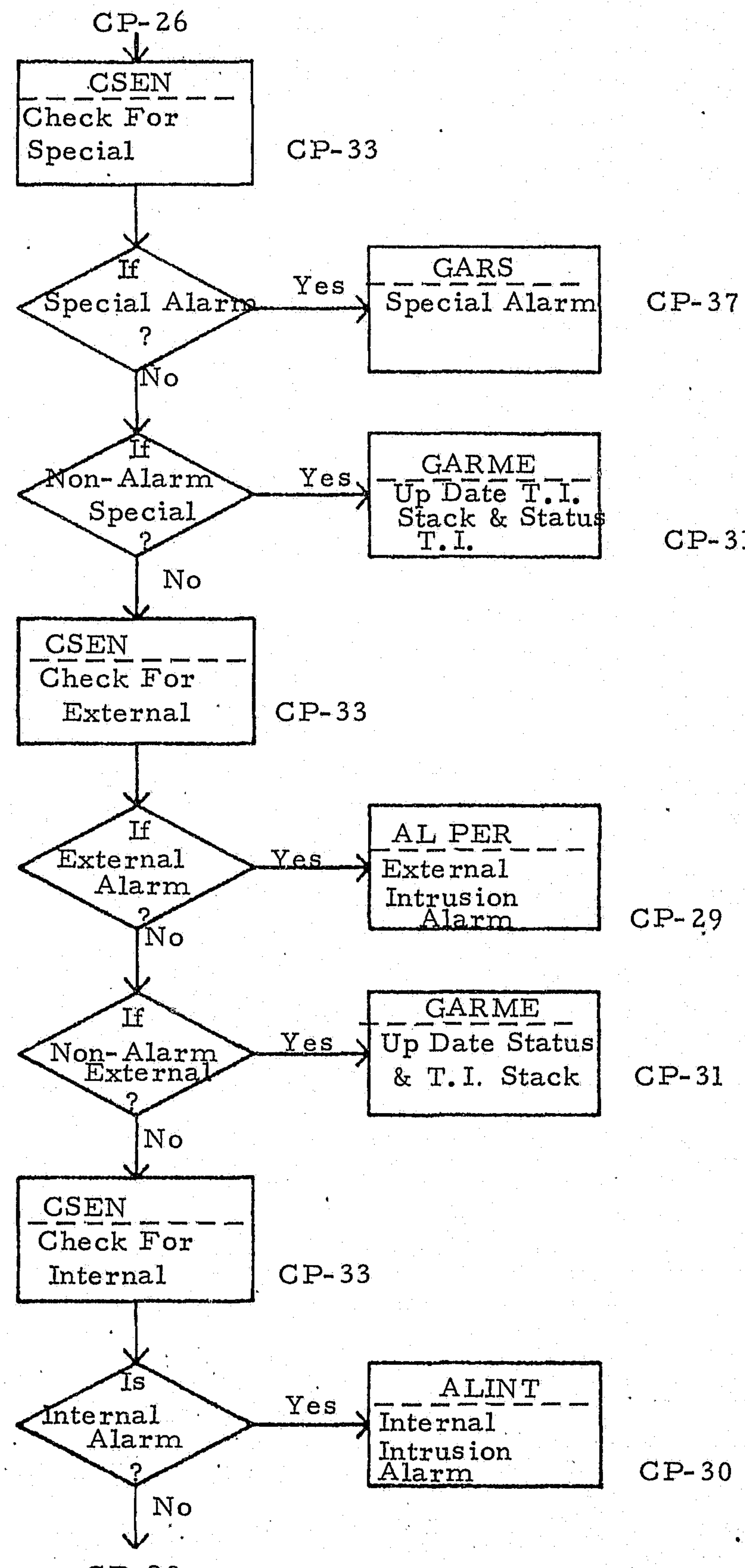

TIERR
Stack T.I. Error Code = T
Set T.I. Bit
If Error Code in stack ?
Yes
Delete Error Code (T) from T.I. Stack
No
Set Pointer At Bottom of T.I. Stack
If T.I. Stack full
No
Store T.I. Error Code
Yes
If T > 100 ?
Yes
Return
No
Find the 1st T.I. Code That is > 100
Replace Old T.I. Code with T
Return

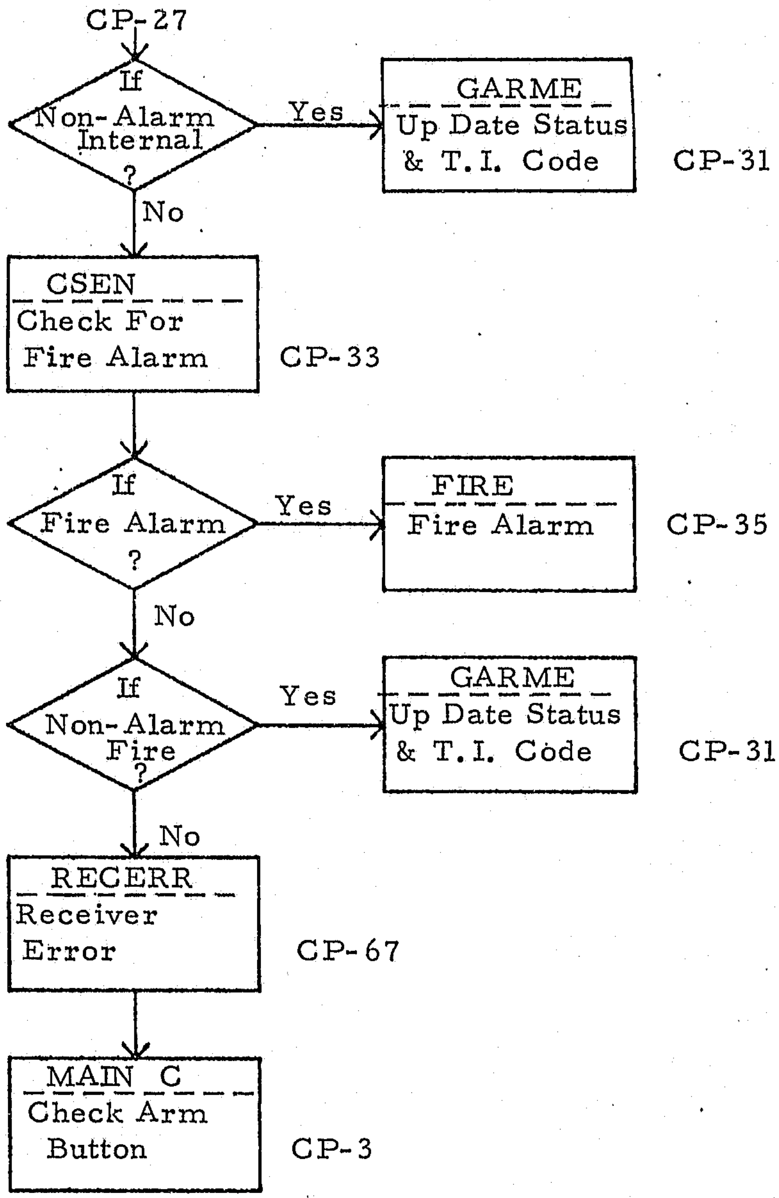

ARMBUT
Armbutton Pressed
If Tamper Disabled ?
Yes
Reset Access Timer & x = 1
No
BCD
Convert T.I. Code from Binary to BCD
CP-25
Output Next T.I. Code
Start Display Timers & Lights
Return

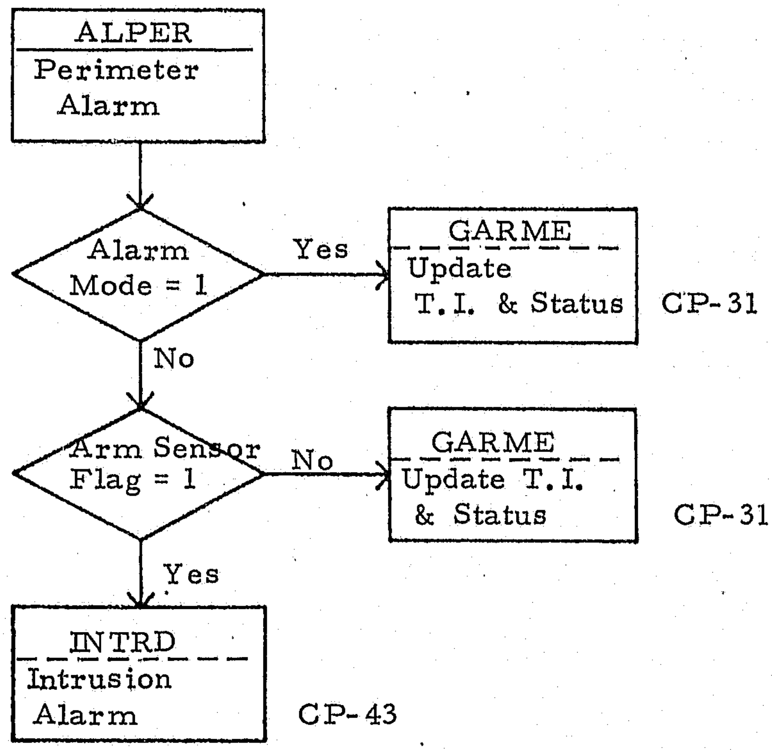

BCD
Binary → BCD
Decimal Adjust & Count No. of 16's
Return

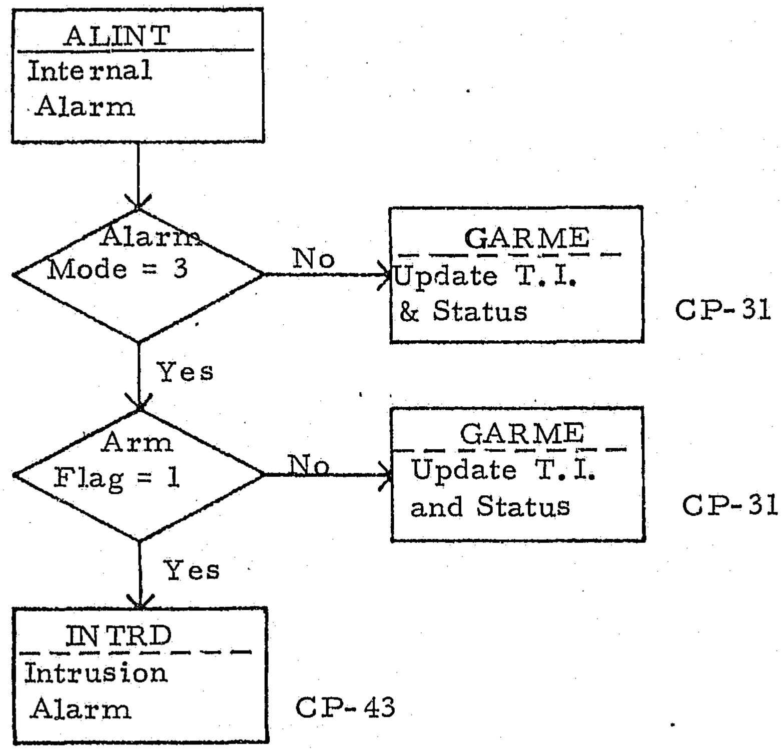

RECDAT
Check Type
Rec. Message
If
E. C.
?
Yes
INEC
Entrance
Control
Message
CP-50
No
CSEN
Check For
Panic Alarm
CP-33
If
Panic Alarm
?
Yes
GARP
Panic Alarm
CP-39
No
If
Non-Alarm
Panic
?
Yes
CARMEE
Up Date
T.I. Stack
CP-32
No
CSEN
Check For
Tamper
CP-33
If
Tamper
Alarm
?
Yes
GART
Tamper Alarm
CP-38
No
If
Non-Alarm
Tamper
?
Yes
GARMEE
Up Date
T.I. Stack
CP-32
No
CP-27

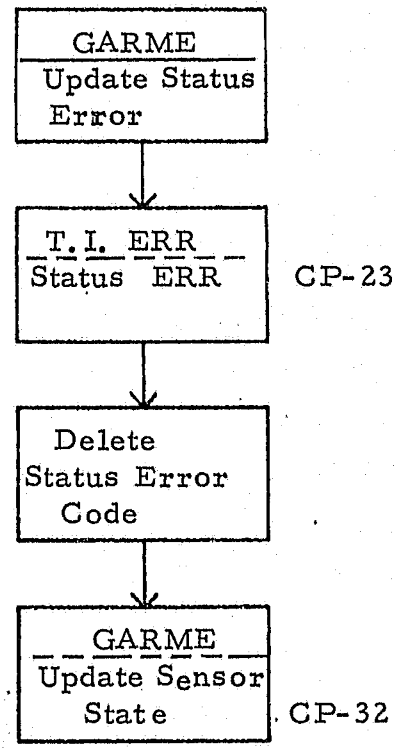
B-28

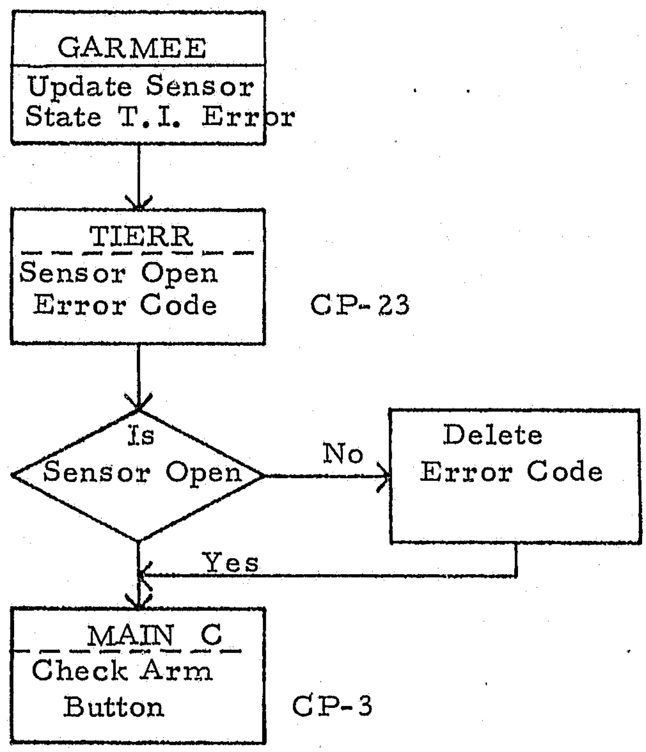

CP-26
CSEN
Check For
Special
CP-33
If
Special Alarm
?
Yes
GARS
Special Alarm
CP-37
No
If
Non-Alarm
Special
?
Yes
GARME
Up Date T.I.
Stack & Status
T.I.
CP-31
No
CSEN
Check For
External
CP-33
If
External
Alarm
?
Yes
AL PER
External
Intrusion
Alarm
CP-29
No
If
Non-Alarm
External
?
Yes
GARME
Up Date Status
& T.I. Stack
CP-31
No
CSEN
Check For
Internal
CP-33
Is
Internal
Alarm
?
Yes
ALINT
Internal
Intrusion
Alarm
CP-30
No
CP-28

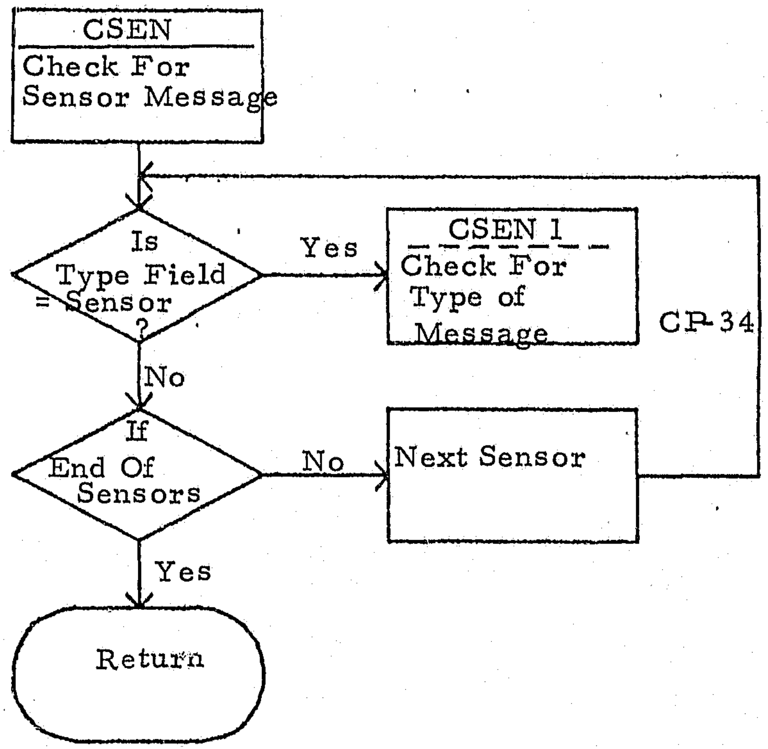

CP-27
If Non-Alarm Internal ?
Yes
GARME
Up Date Status & T.I. Code
CP-31
No
CSEN
Check For Fire Alarm
CP-33
If Fire Alarm ?
Yes
FIRE
Fire Alarm
CP-35
No
If Non-Alarm Fire ?
Yes
GARME
Up Date Status & T.I. Code
CP-31
No
RECERR
Receiver Error
CP-67
MAIN C
Check Arm Button
CP-3

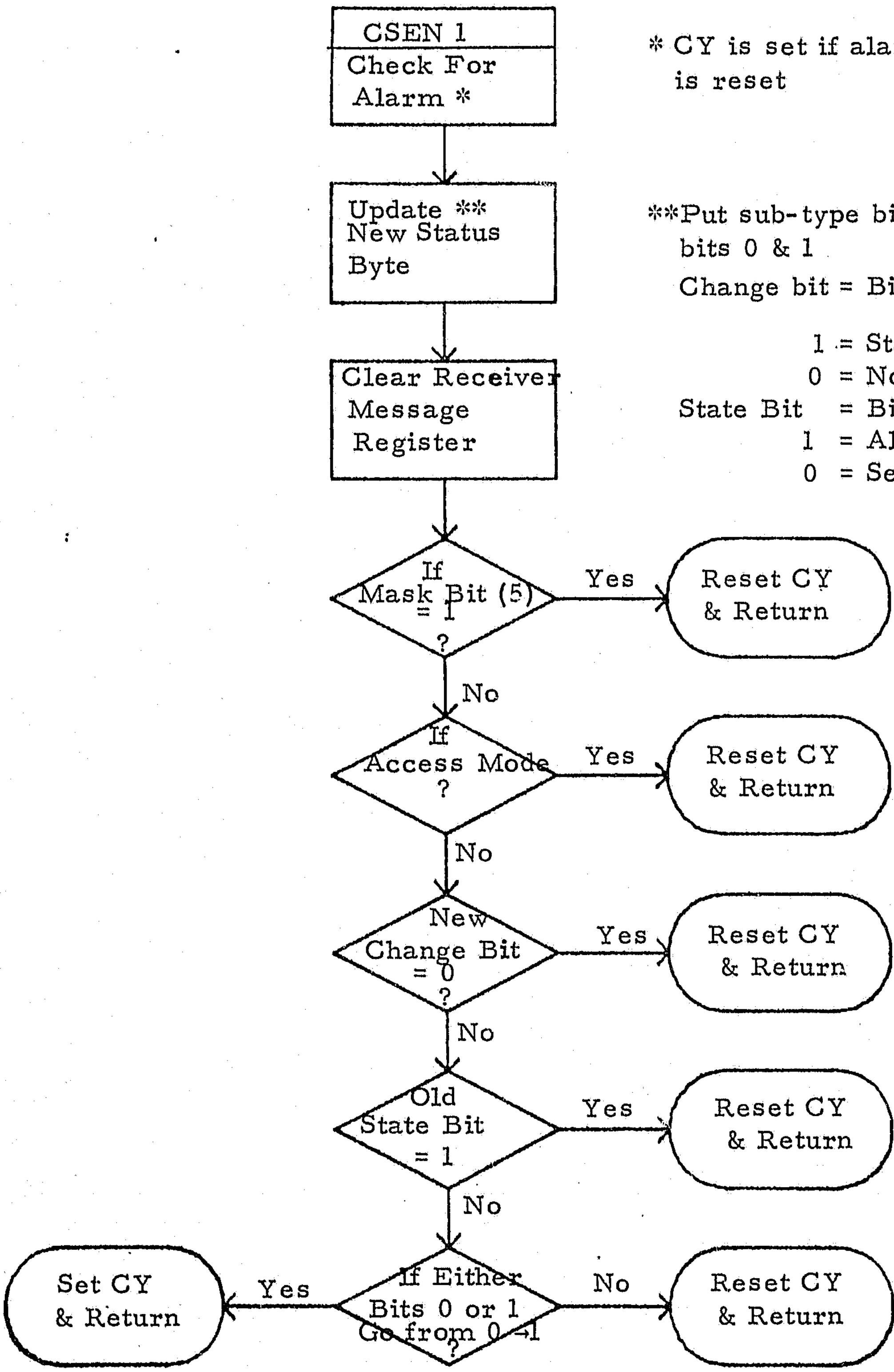

ALPER
Perimeter Alarm
Alarm Mode = 1
Yes
GARME
Update T.I. & Status
CP-31
No
Arm Sensor Flag = 1
No
GARME
Update T.I. & Status
CP-31
Yes
INTRD
Intrusion Alarm
CP-43


ALINT
Internal Alarm
Alarm Mode = 3
No
GARME
Update T.I. & Status
CP-31
Yes
Arm Flag = 1
No
GARME
Update T.I. and Status
CP-31
Yes
INTRD
Intrusion Alarm
CP-43


GARME
Update Status Error
T.I. ERR
Status ERR
CP-23
Delete Status Error Code
GARME
Update Sensor State
CP-32


GARMEE
Update Sensor State T.I. Error
TIERR
Sensor Open Error Code
CP-23
Is Sensor Open
No
Delete Error Code
Yes
MAIN C
Check Arm Button
CP-3


CSEN
Check For Sensor Message
Is Type Field = Sensor ?
Yes
CSEN 1
Check For Type of Message
CP-34
No
If End Of Sensors
No
Next Sensor
Yes
Return



* CY is set if alarm else CY is reset

**Put sub-type bits in status bits 0 & 1

Change bit = Bit 1

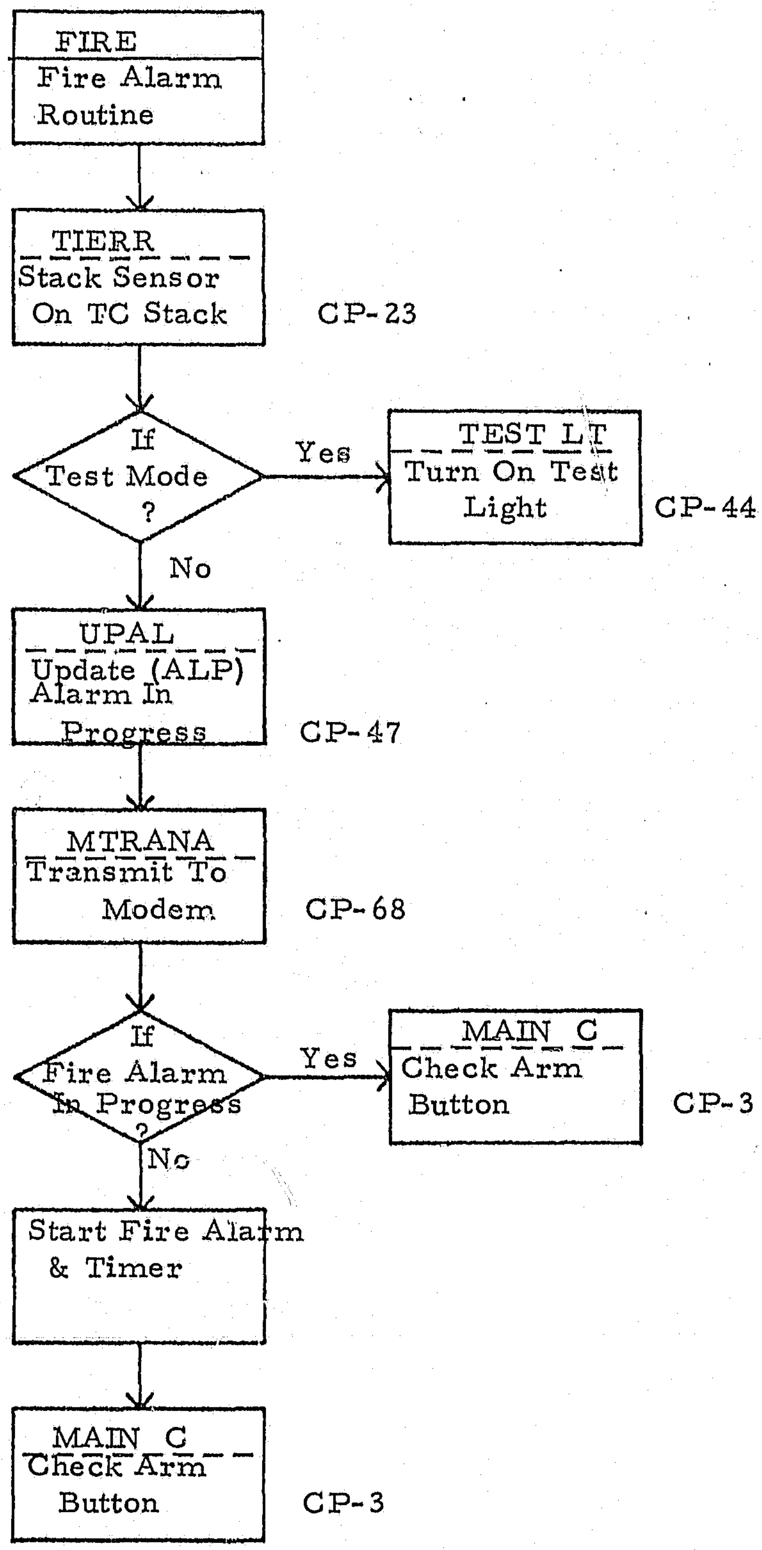
1 = State Change

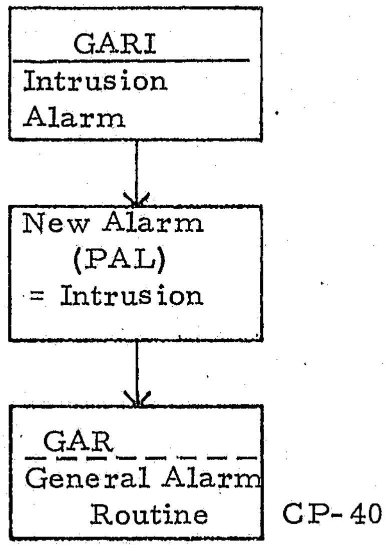
0 = No Change

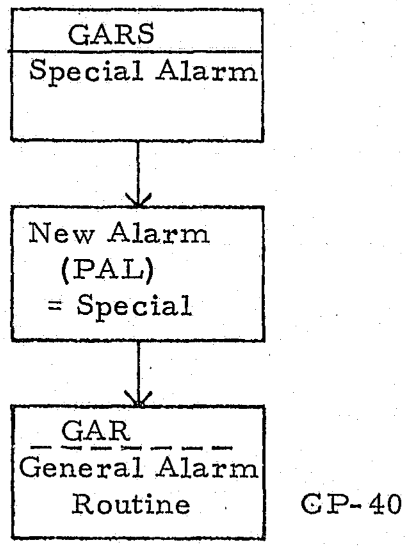
State Bit = Bit 0

1 = Alarm

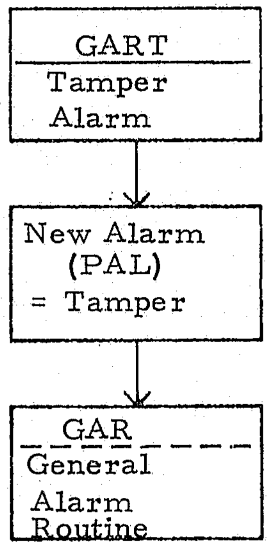
0 = Secure


FIRE
Fire Alarm Routine
TIERR
Stack Sensor On TC Stack
CP-23
If Test Mode ?
Yes
TEST LT
Turn On Test Light
CP-44
No
UPAL
Update (ALP) Alarm In Progress
CP-47
MTRANA
Transmit To Modem
CP-68
If Fire Alarm In Progress ?
Yes
MAIN C
Check Arm Button
CP-3
No
Start Fire Alarm & Timer
MAIN C
Check Arm Button
CP-3

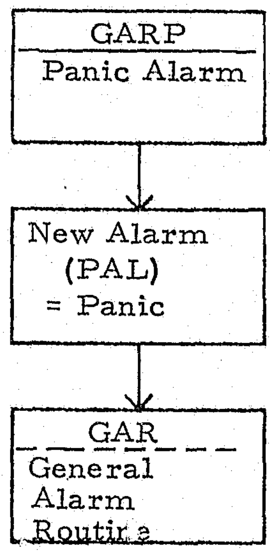

GARI
Intrusion Alarm
New Alarm (PAL) = Intrusion
GAR
General Alarm Routine
CP-40


GARS
Special Alarm
New Alarm
(PAL)
= Special
GAR
General Alarm
Routine
CP-40

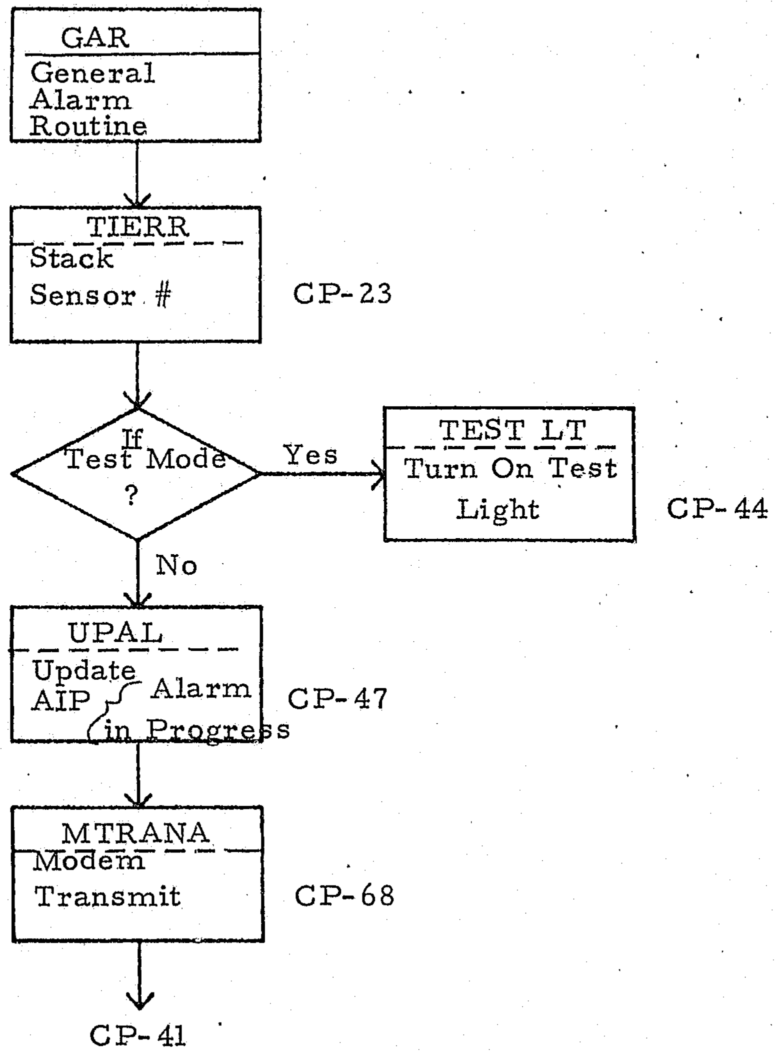
CP-37

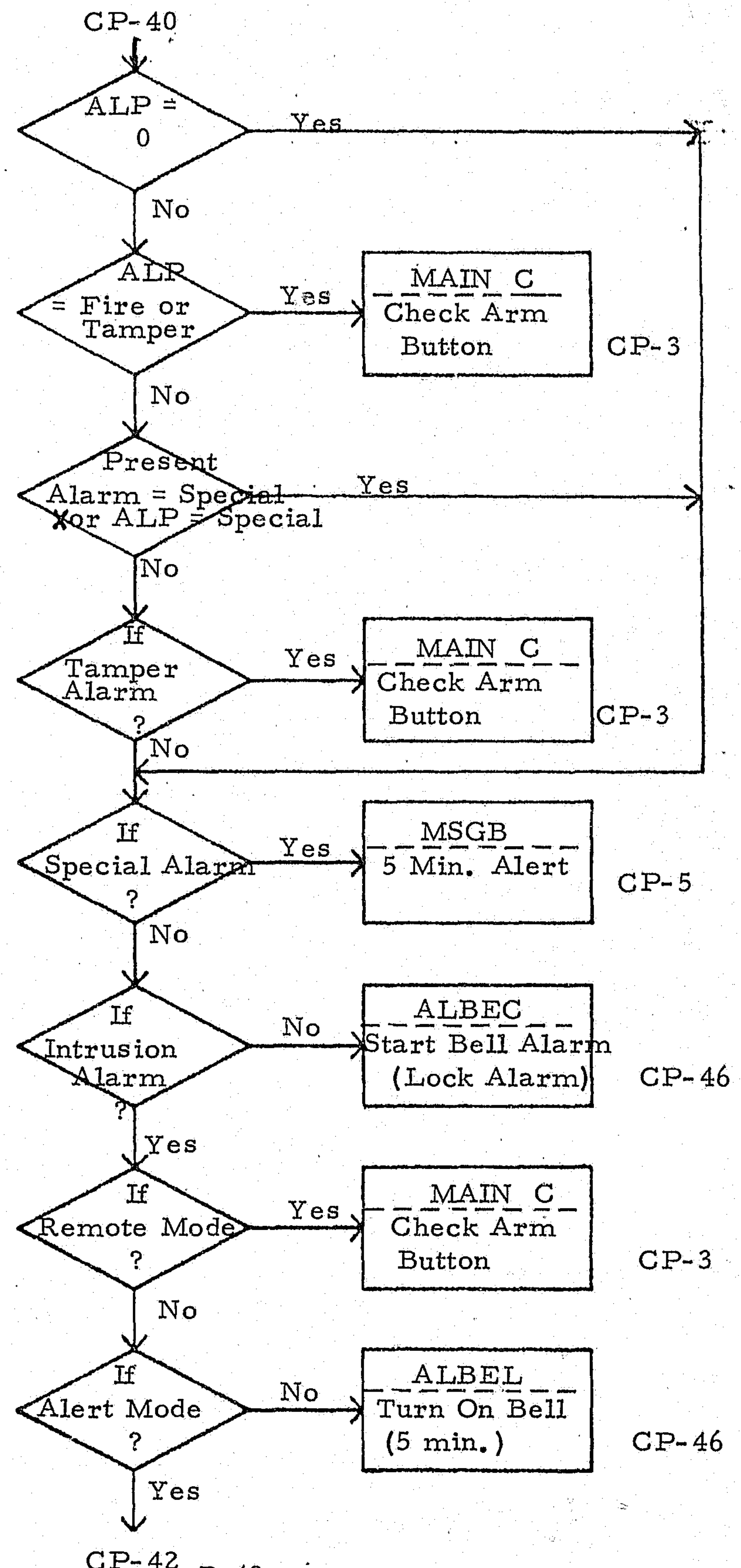

GART
Tamper
Alarm
New Alarm
(PAL)
= Tamper
GAR
General
Alarm
Routine

CP-40


GARP
Panic Alarm
New Alarm (PAL) = Panic
GAR
General Alarm Routine

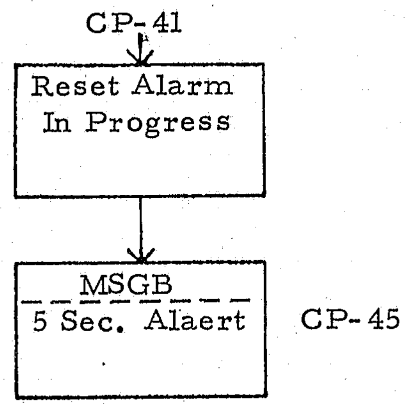
CP-40

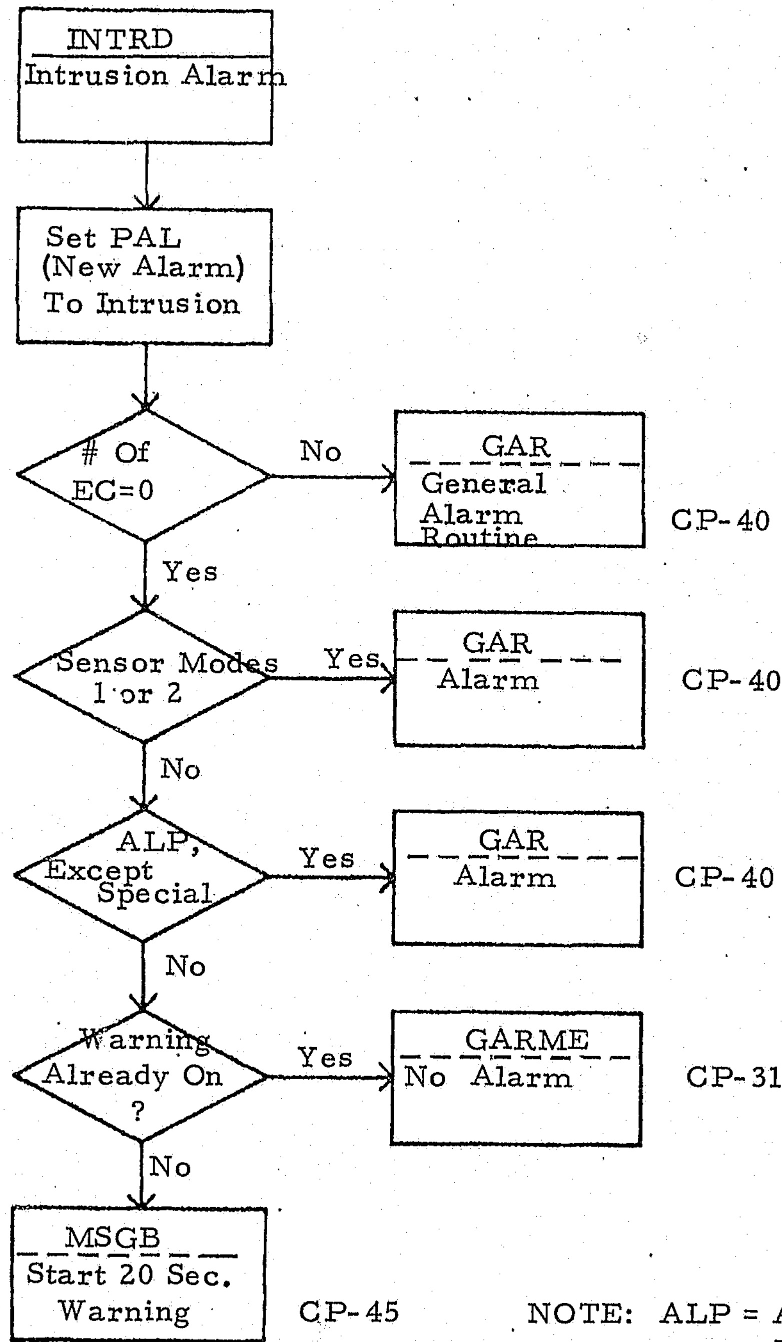

GAR
General Alarm Routine
TIERR
Stack Sensor #
CP-23
If Test Mode ?
Yes
TEST LT
Turn On Test Light
CP-44
No
UPAL
Update AIP Alarm in Progress
CP-47
MTRANA
Modem Transmit
CP-68
CP-41



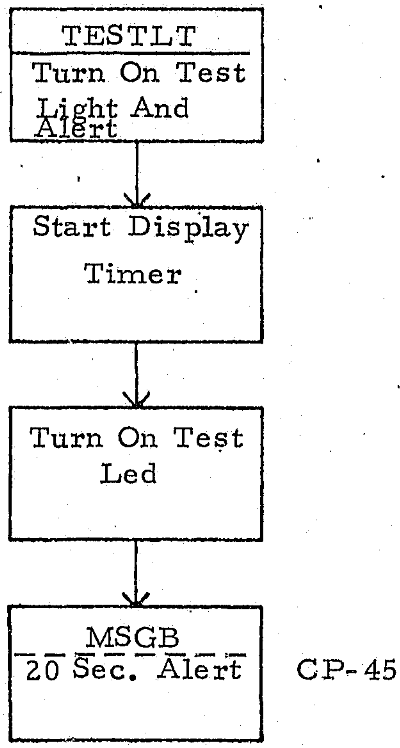
CP-40
ALP = 0
Yes
No
ALP = Fire or Tamper
Yes
MAIN C
Check Arm Button
CP-3
No
Present Alarm = Special Xor ALP = Special
Yes
No
If Tamper Alarm ?
Yes
MAIN C
Check Arm Button
CP-3
No
If Special Alarm ?
Yes
MSGB
5 Min. Alert
CP-5
No
If Intrusion Alarm ?
No
ALBEC
Start Bell Alarm (Lock Alarm)
CP-46
Yes
If Remote Mode ?
Yes
MAIN C
Check Arm Button
CP-3
No
If Alert Mode ?
No
ALBEL
Turn On Bell (5 min.)
CP-46
Yes
CP-42

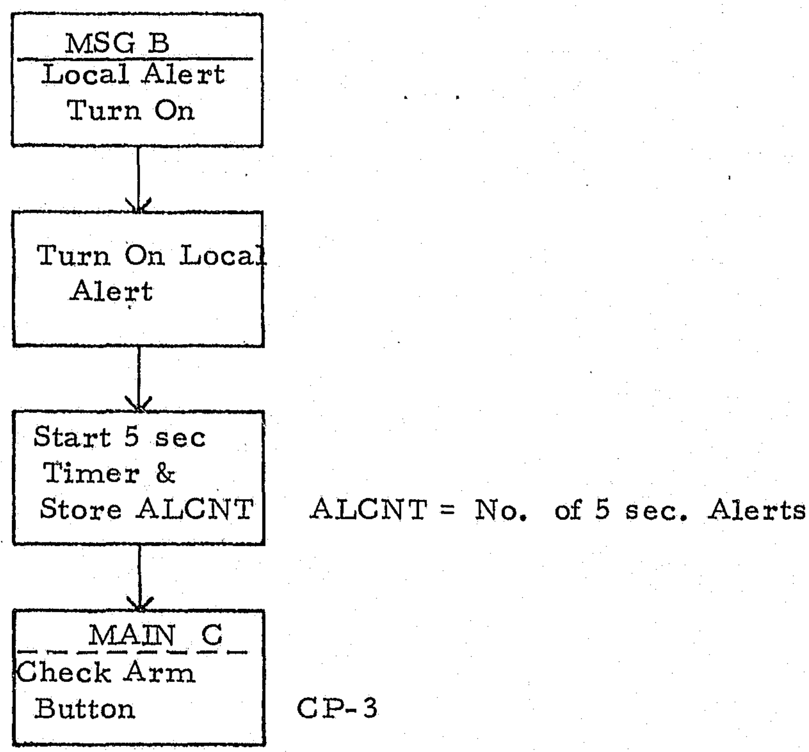
CP-41

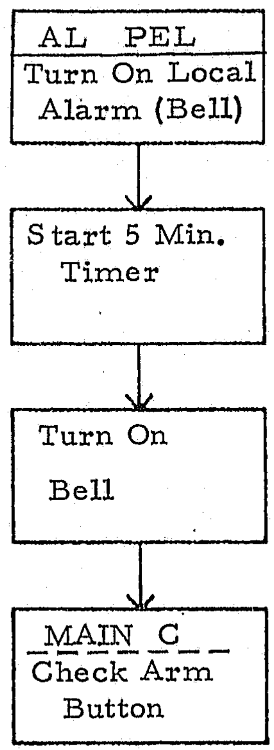

CP-41
Reset Alarm In Progress
MSGB
5 Sec. Alaert
CP-45



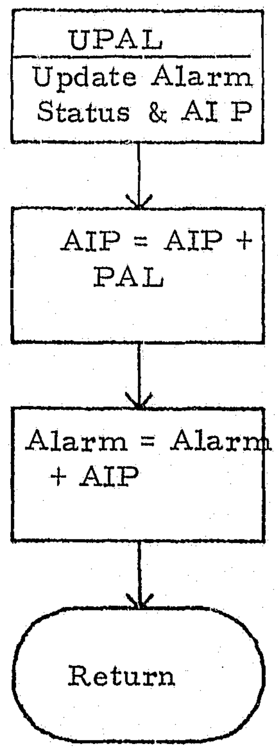
NOTE: ALP = Alarm In Progress


TESTLT
Turn On Test Light And Alert
Start Display Timer
Turn On Test Led
MSGB
20 Sec. Alert
CP-45


MSG B
Local Alert
Turn On
Turn On Local
Alert
Start 5 sec
Timer &
Store ALCNT
ALCNT = No. of 5 sec. Alerts
MAIN C
Check Arm
Button
CP-3

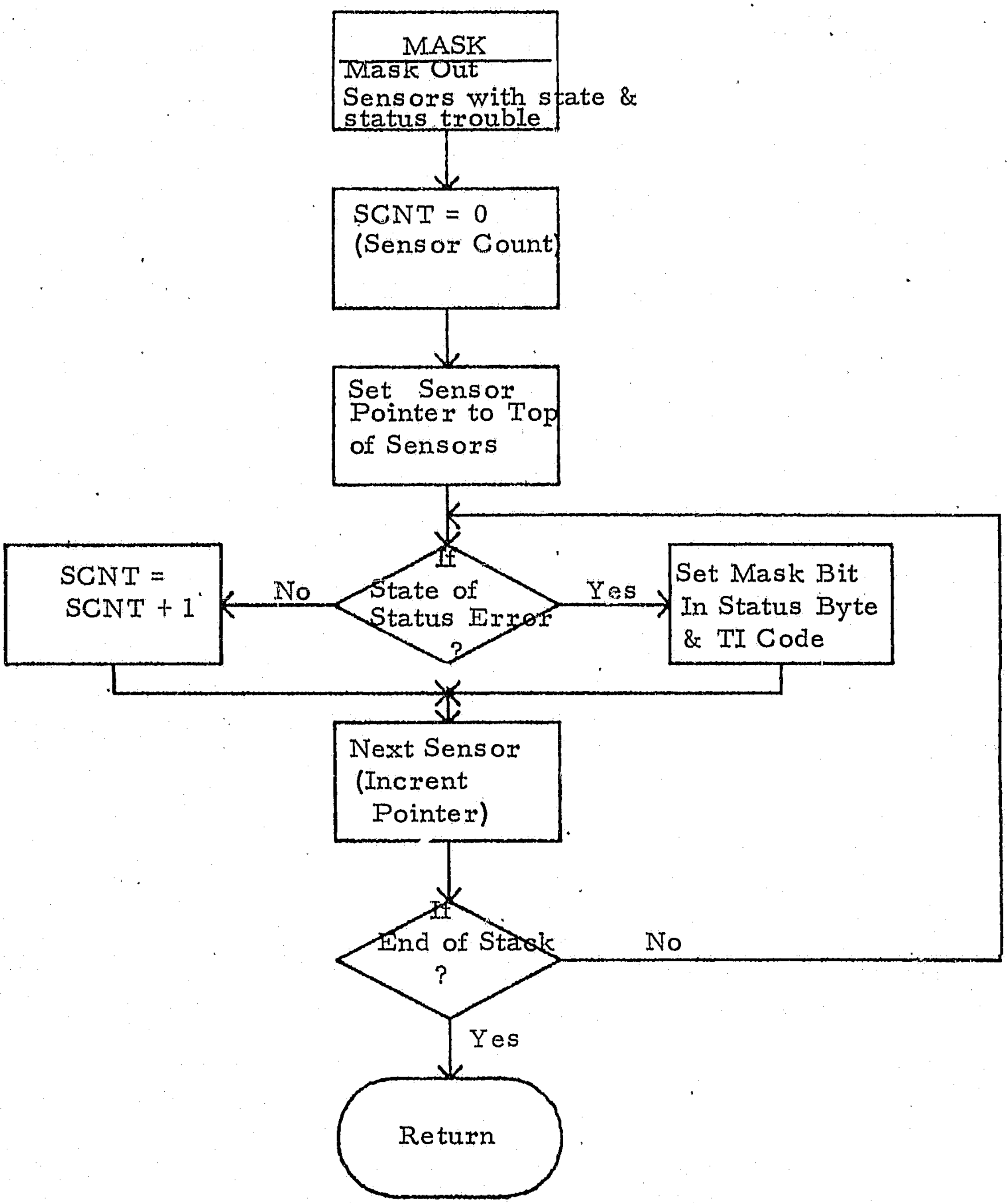

AL PEL
Turn On Local Alarm (Bell)
Start 5 Min. Timer
Turn On Bell
MAIN C
Check Arm Button

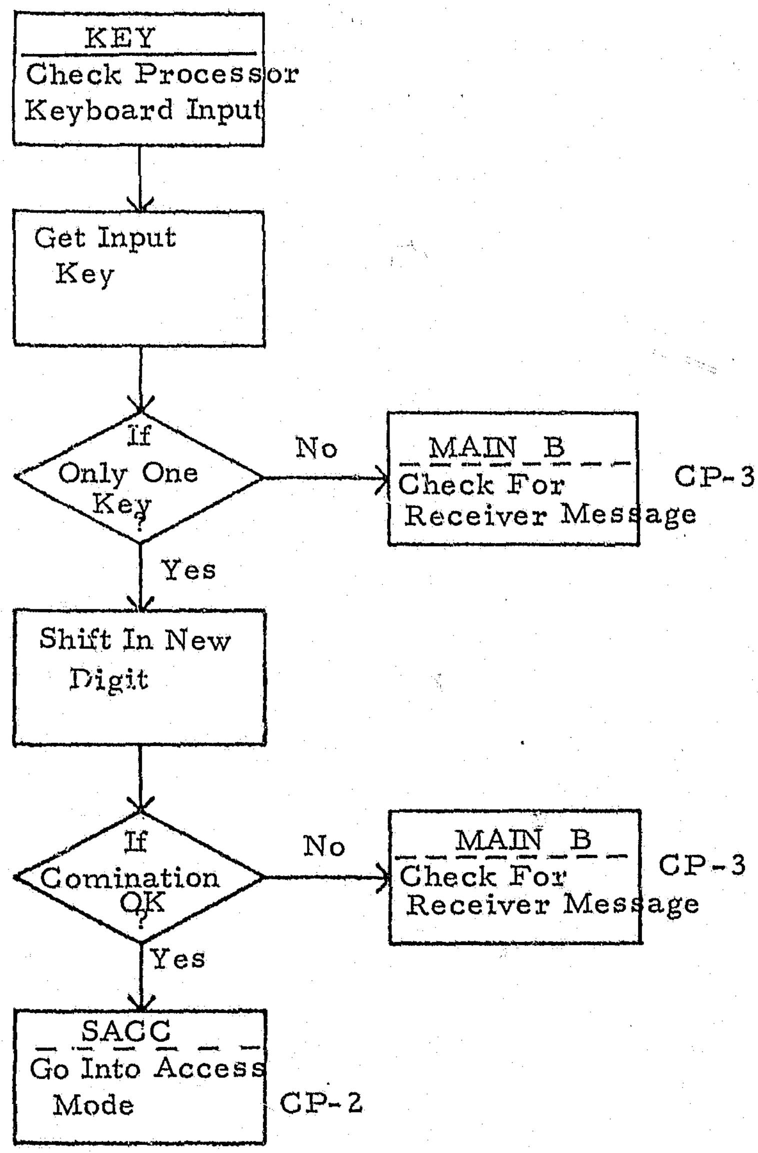
CP-3

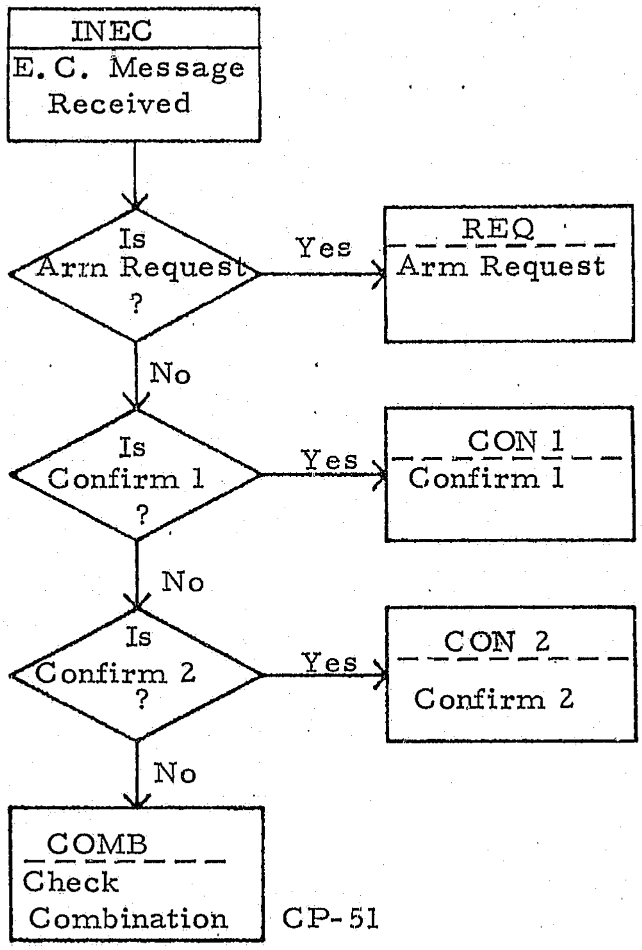


ALP = Alarm In Progress

PAL = Present Alarm


MASK
Mask Out
Sensors with state & status trouble
SCNT = 0
(Sensor Count)
Set Sensor Pointer to Top of Sensors
SCNT = SCNT + 1
No
If State of Status Error ?
Yes
Set Mask Bit In Status Byte & TI Code
Next Sensor (Incrent Pointer)
If End of Stack ?
No
Yes
Return


KEY
Check Processor Keyboard Input
Get Input Key
If Only One Key ?
No
MAIN B
Check For Receiver Message
CP-3
Yes
Shift In New Digit
If Comination OK ?
No
MAIN B
Check For Receiver Message
CP-3
Yes
SACC
Go Into Access Mode
CP-2

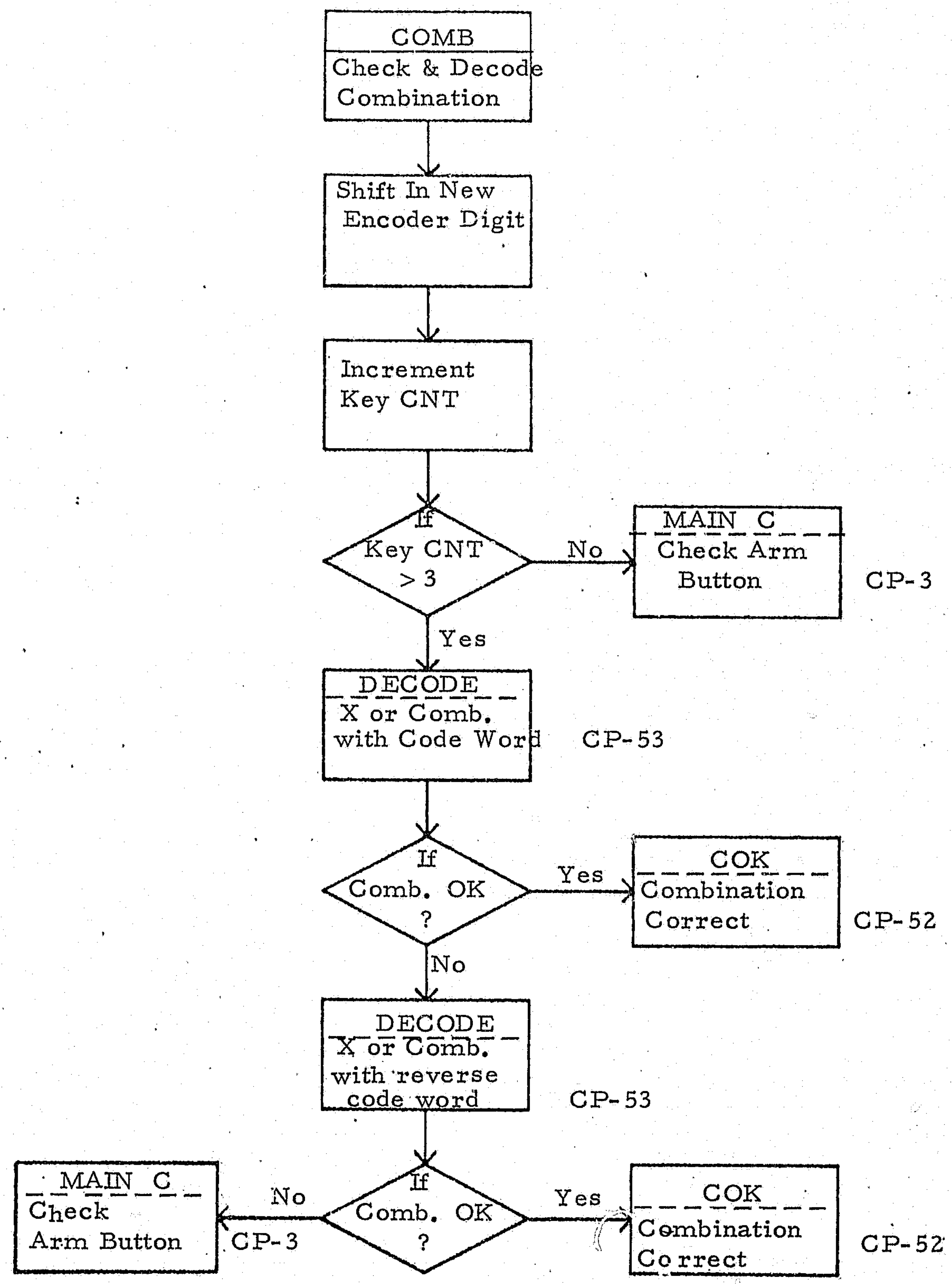


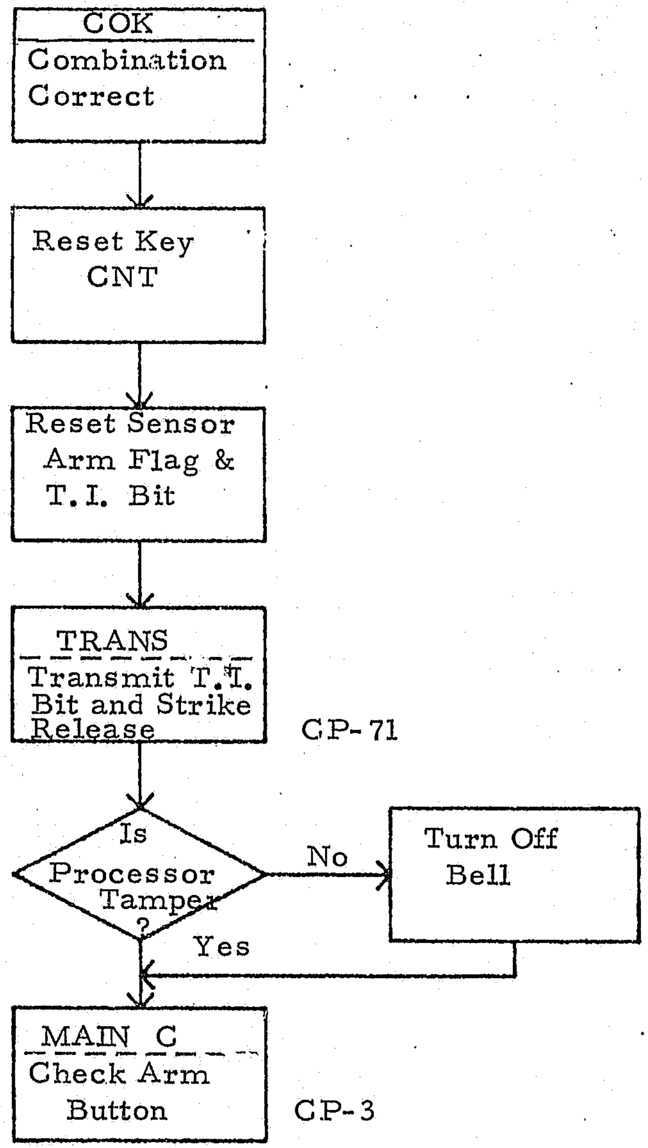
CP-56

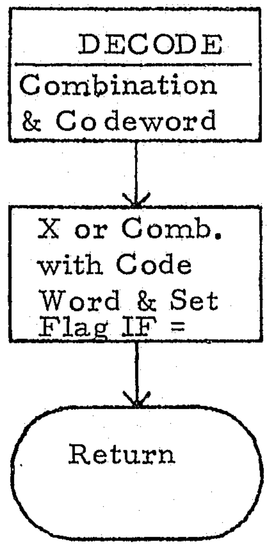
CP-57

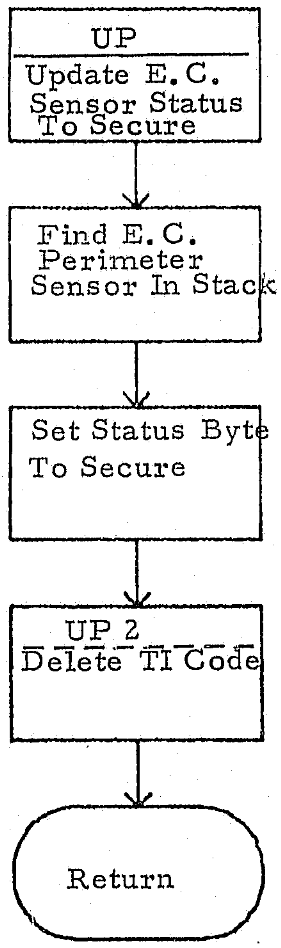
CP-58

CP-51

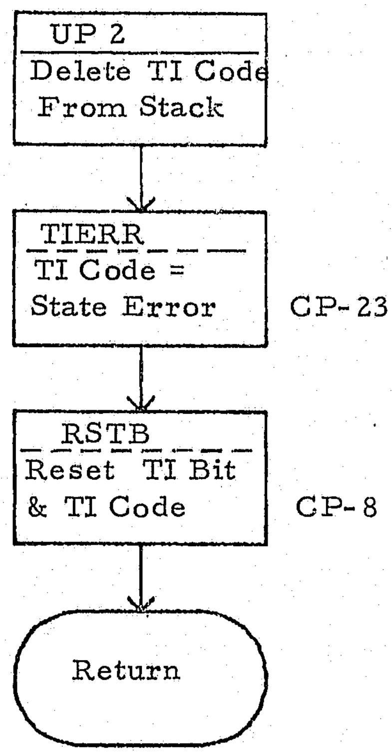

COMB
Check & Decode Combination
Shift In New Encoder Digit
Increment Key CNT
If Key CNT > 3
No
MAIN C
Check Arm Button
CP-3
Yes
DECODE
X or Comb. with Code Word
CP-53
If Comb. OK ?
Yes
COK
Combination Correct
CP-52
No
DECODE
X or Comb. with reverse code word
CP-53
If Comb. OK ?
No
MAIN C
Check Arm Button
CP-3
Yes
COK
Combination Correct
CP-52

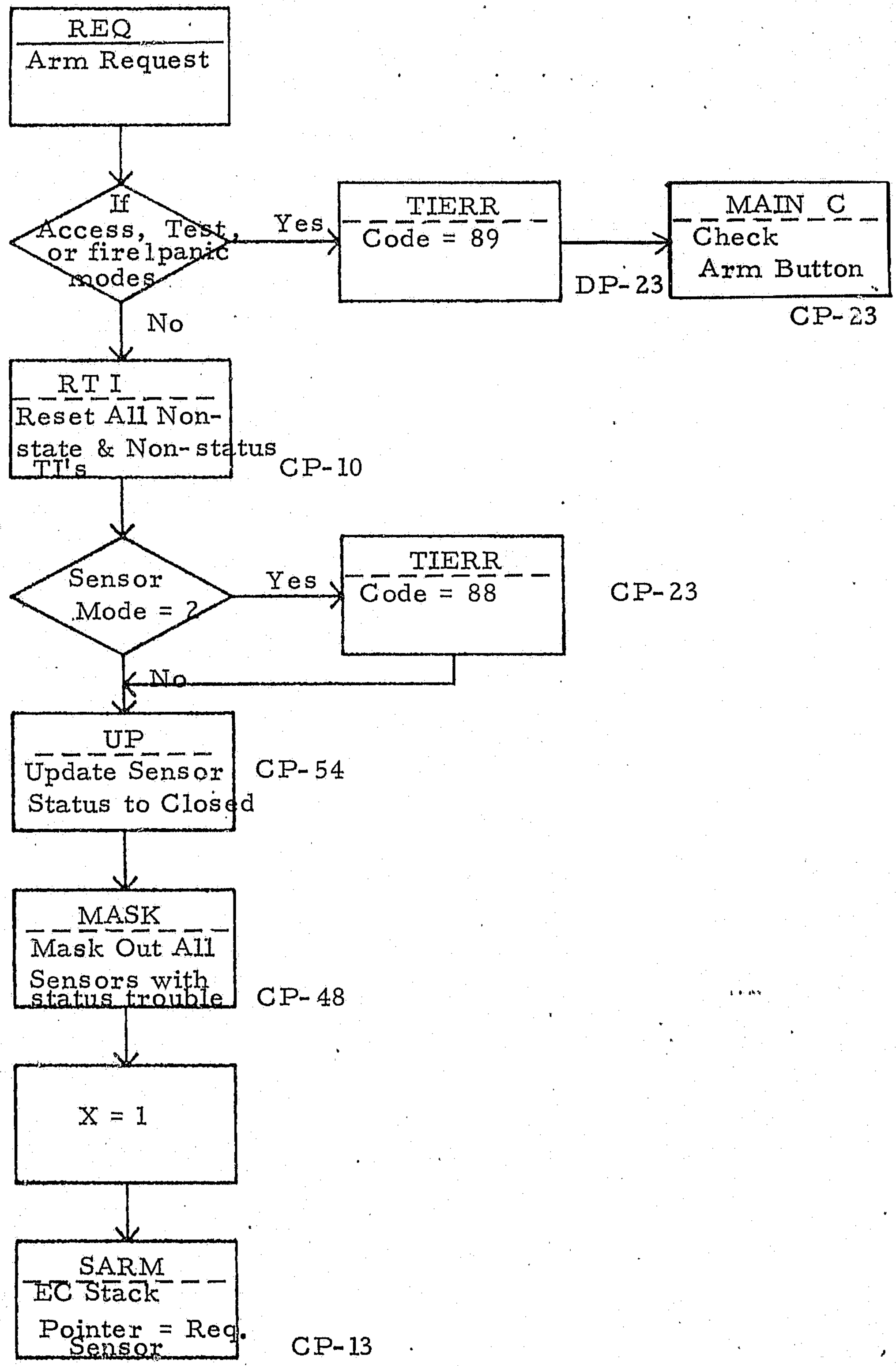

COK
Combination Correct
Reset Key CNT
Reset Sensor Arm Flag & T.I. Bit
TRANS
Transmit T.I. Bit and Strike Release
CP-71
Is Processor Tamper ?
No
Turn Off Bell
Yes
MAIN C
Check Arm Button
CP-3

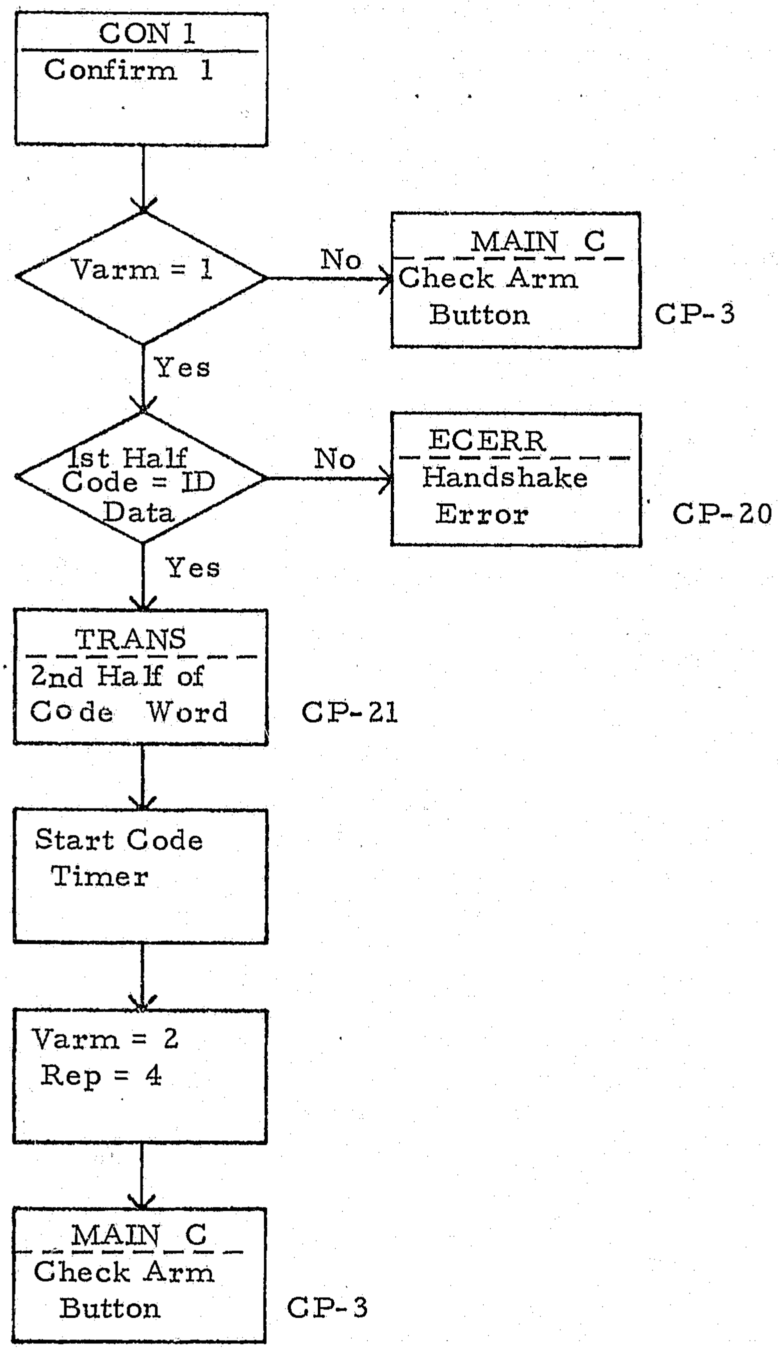

DECODE
Combination
& Codeword
X or Comb.
with Code
Word & Set
Flag IF =
Return

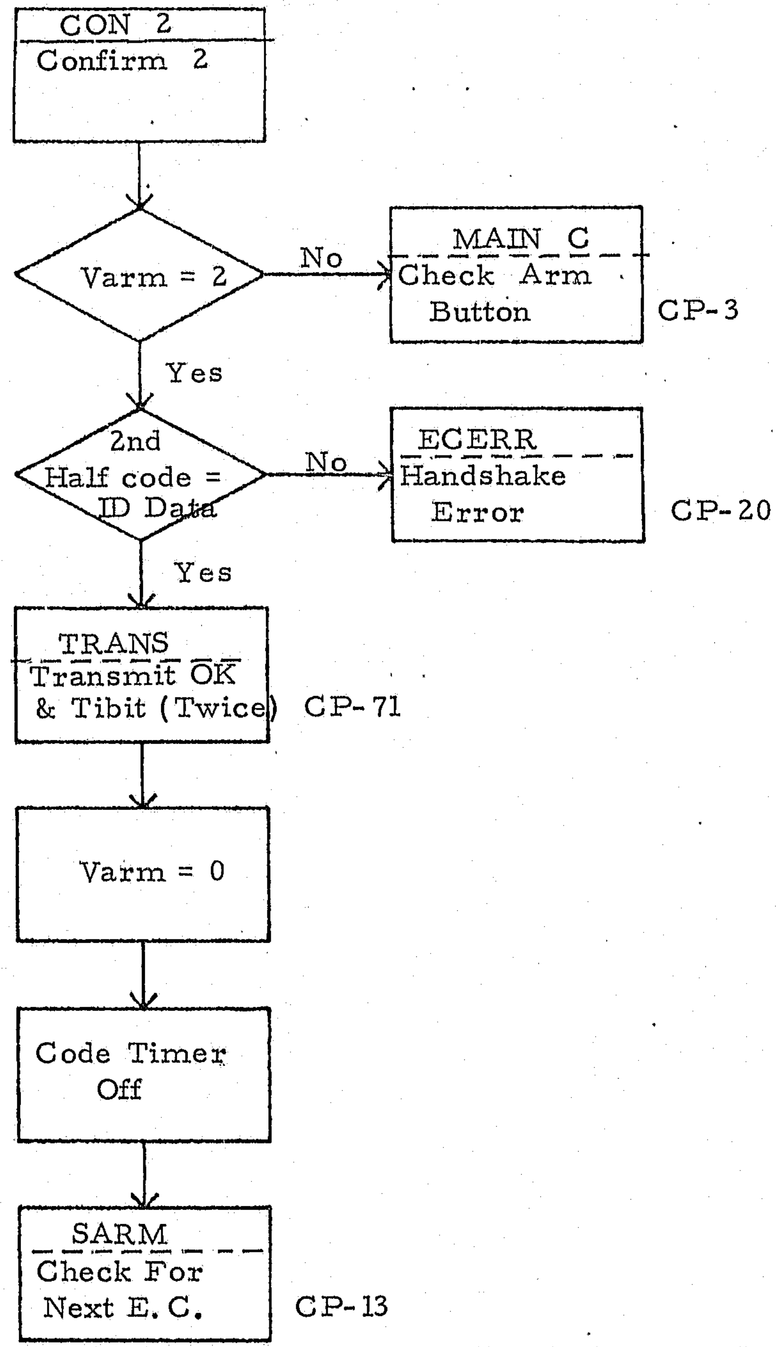

UP
Update E.C. Sensor Status To Secure
Find E.C. Perimeter Sensor In Stack
Set Status Byte To Secure
UP 2
Delete TI Code
Return

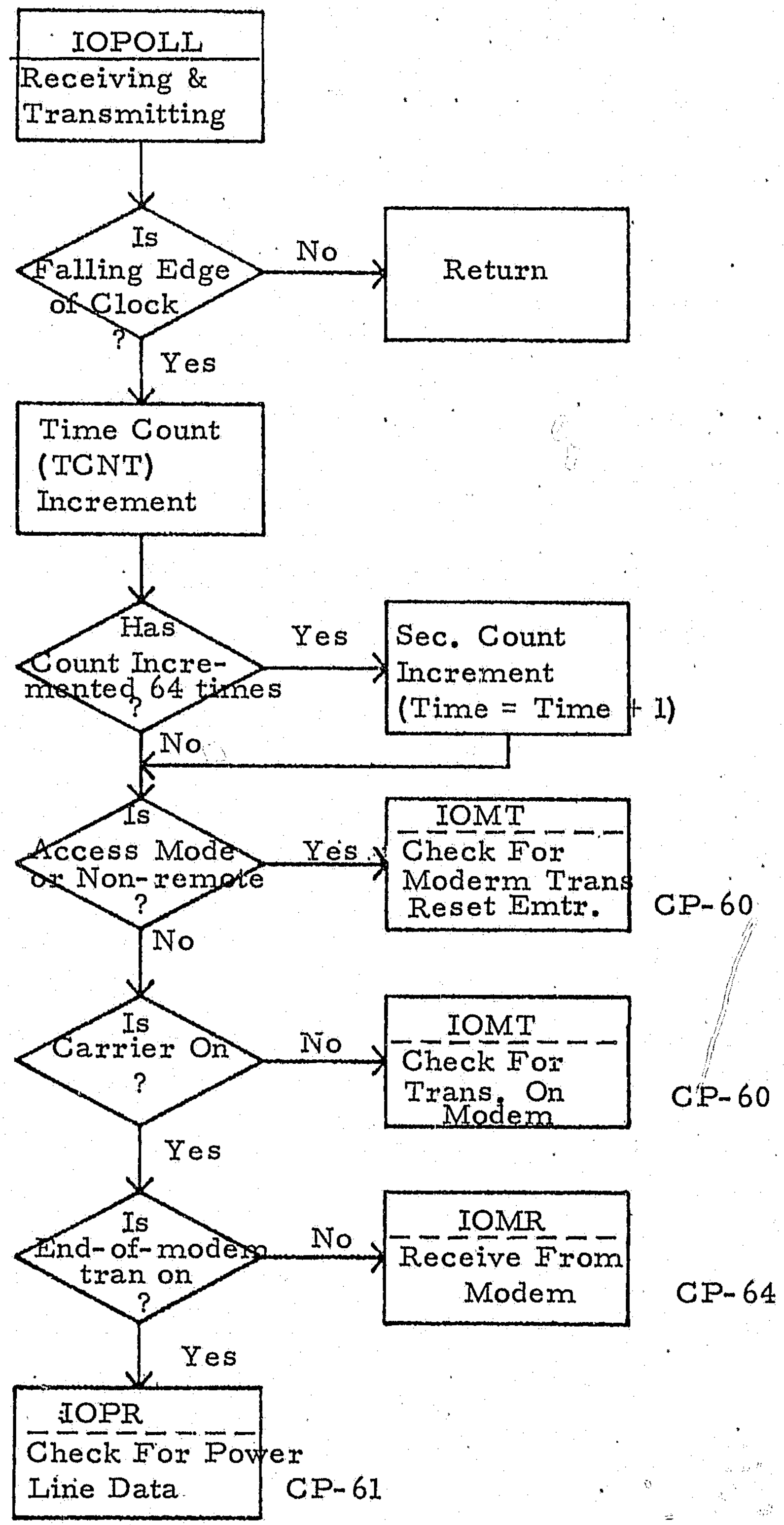
CP-55

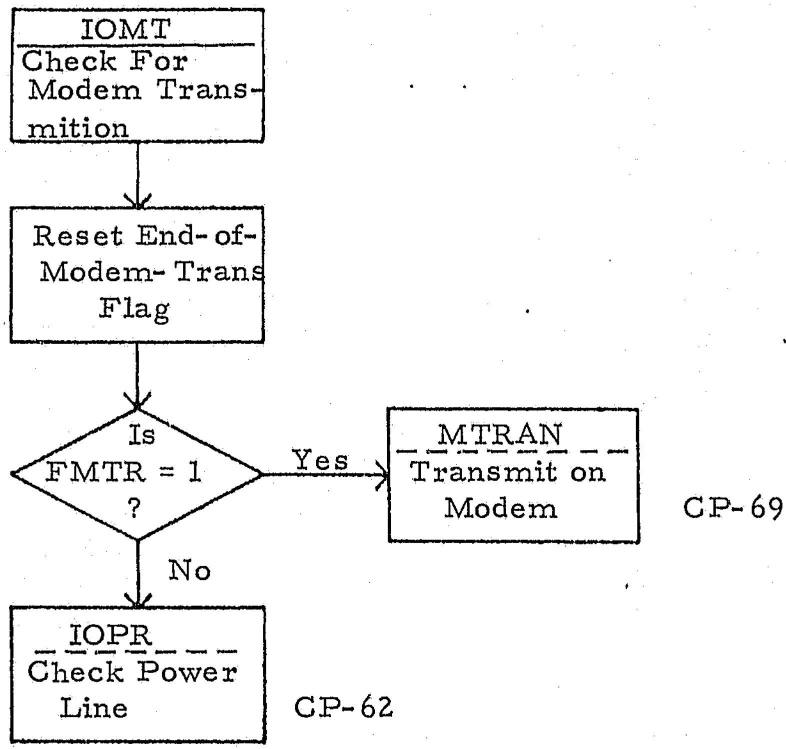

UP 2
Delete TI Code From Stack
TIERR
TI Code = State Error
CP-23
RSTB
Reset TI Bit & TI Code
CP-8
Return

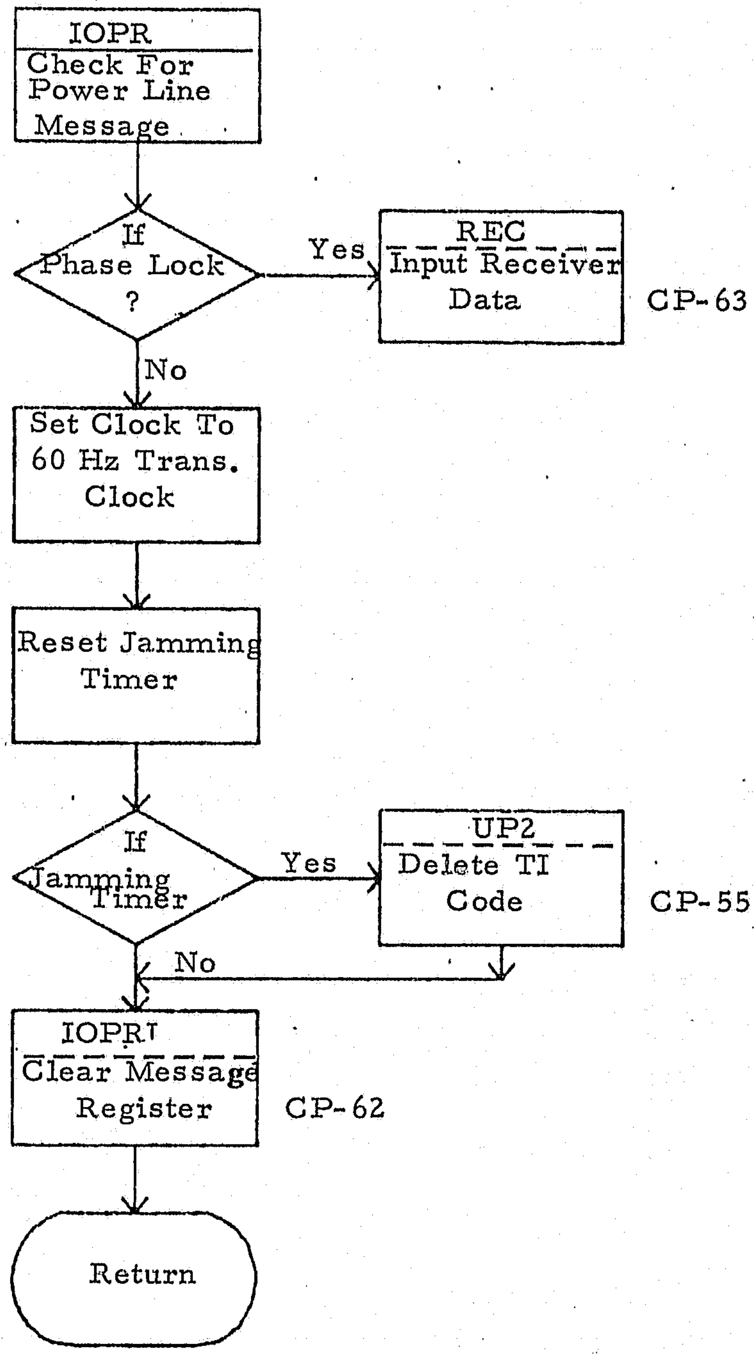

REQ
Arm Request
If Access, Test, or fire/panic modes
Yes
No
TIERR
Code = 89
DP-23
MAIN C
Check Arm Button
CP-23
RTI
Reset All Non-state & Non-status TI's
CP-10
Sensor Mode = 2
Yes
No
TIERR
Code = 88
CP-23
UP
Update Sensor Status to Closed
CP-54
MASK
Mask Out All Sensors with status trouble
CP-48
X = 1
SARM
EC Stack Pointer = Req. Sensor
CP-13

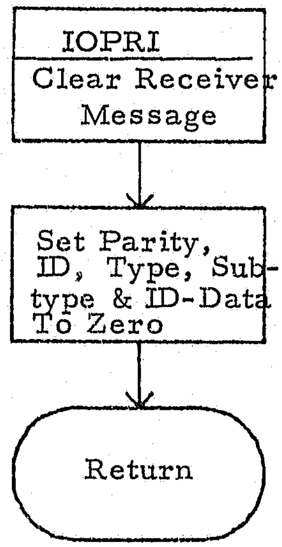

CON 1
Confirm 1
Varm = 1
No
MAIN C
Check Arm
Button
CP-3
Yes
Ist Half
Code = ID
Data
No
ECERR
Handshake
Error
CP-20
Yes
TRANS
2nd Half of
Code Word
CP-21
Start Code
Timer
Varm = 2
Rep = 4
MAIN C
Check Arm
Button
CP-3

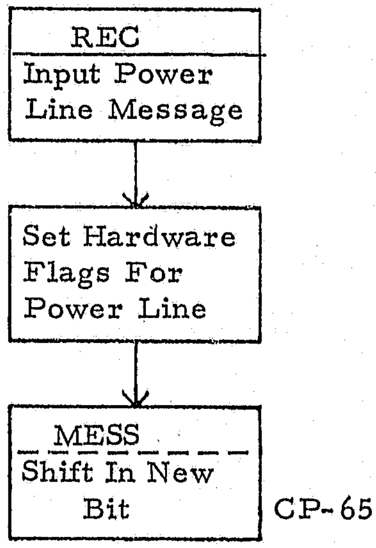

CON 2
Confirm 2
Varm = 2
No
MAIN C
Check Arm
Button
CP-3
Yes
2nd
Half code =
ID Data
No
ECERR
Handshake
Error
CP-20
Yes
TRANS
Transmit OK
& Tibit (Twice)
CP-71
Varm = 0
Code Timer
Off
SARM
Check For
Next E. C.
CP-13

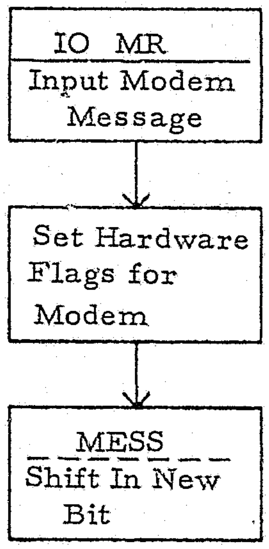

IOPOLL
Receiving & Transmitting
Is Falling Edge of Clock ?
No
Return
Yes
Time Count (TCNT) Increment
Has Count Incre- mented 64 times ?
Yes
Sec. Count Increment (Time = Time + 1)
No
Is Access Mode or Non-remote ?
Yes
IOMT
Check For Moderm Trans Reset Emtr.
CP-60
No
Is Carrier On ?
No
IOMT
Check For Trans. On Modem
CP-60
Yes
Is End-of-modem tran on ?
No
IOMR
Receive From Modem
CP-64
Yes
IOPR
Check For Power Line Data
CP-61


IOMT
Check For Modem Transmition
Reset End-of-Modem-Trans Flag
Is FMTR = 1 ?
Yes
MTRAN
Transmit on Modem
CP-69
No
IOPR
Check Power Line
CP-62

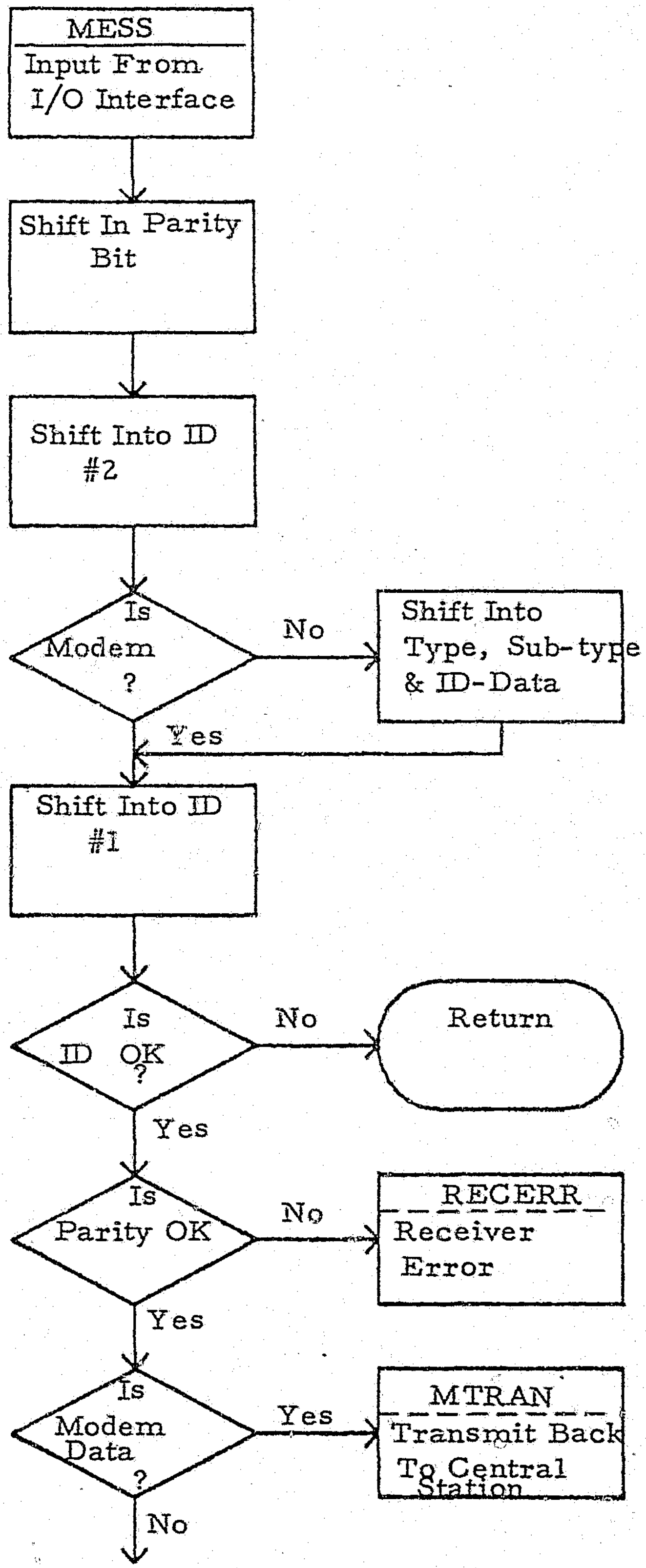

IOPR
Check For Power Line Message
If Phase Lock ?
Yes
REC
Input Receiver Data
CP-63
No
Set Clock To 60 Hz Trans. Clock
Reset Jamming Timer
If Jamming Timer
Yes
UP2
Delete TI Code
CP-55
No
IOPRT
Clear Message Register
CP-62
Return


IOPRI
Clear Receiver Message
Set Parity, ID, Type, Sub-type & ID-Data To Zero
Return


REC
Input Power Line Message
Set Hardware Flags For Power Line
MESS
Shift In New Bit
CP-65


IO MR
Input Modem Message
Set Hardware Flags for Modem
MESS
Shift In New Bit

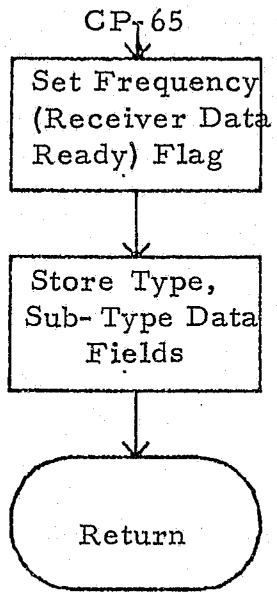
CP-65

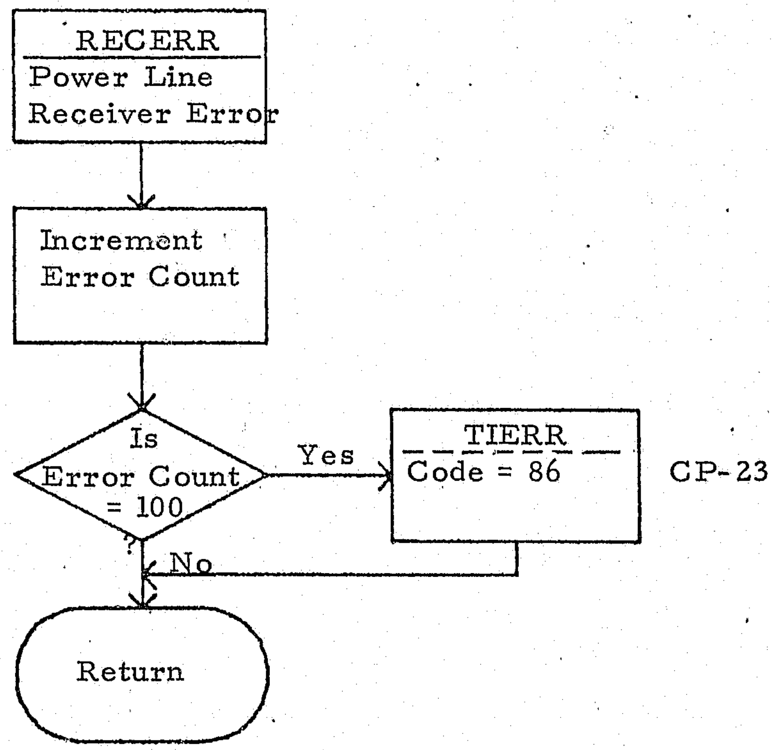


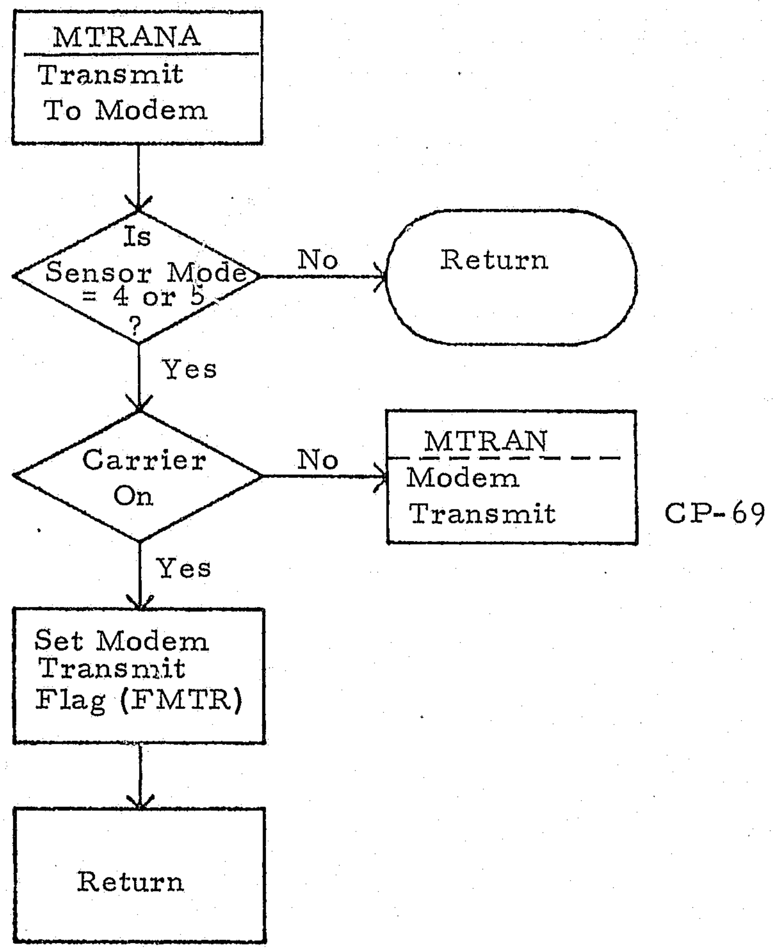
CP-67

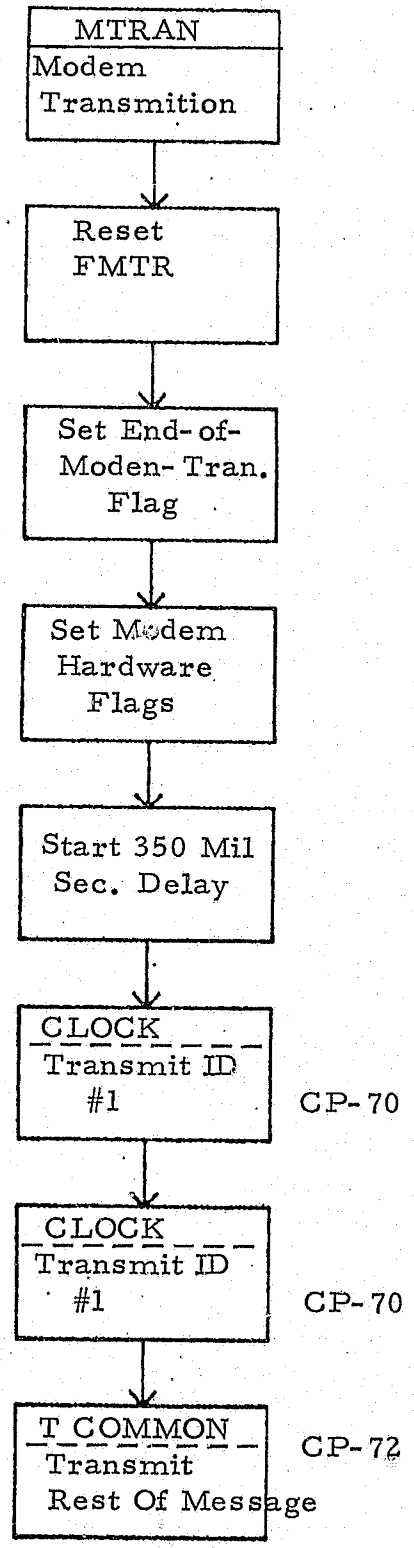
CP-69

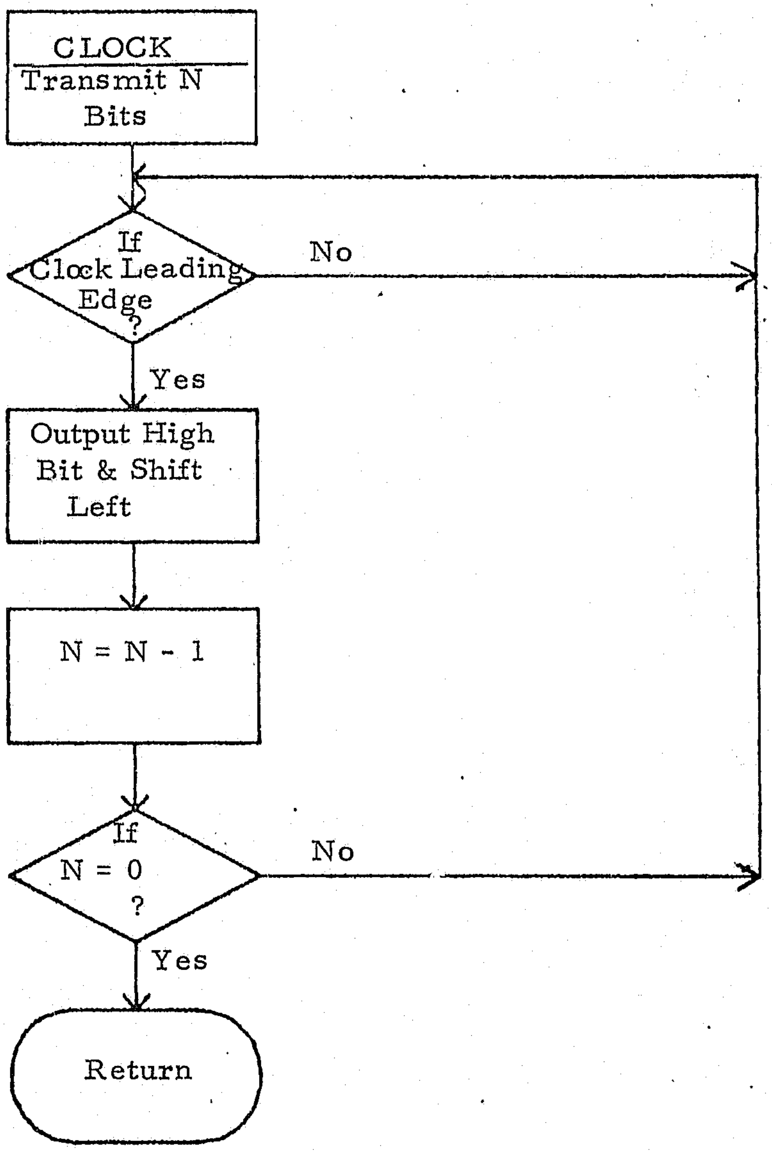
CP-66 B-67

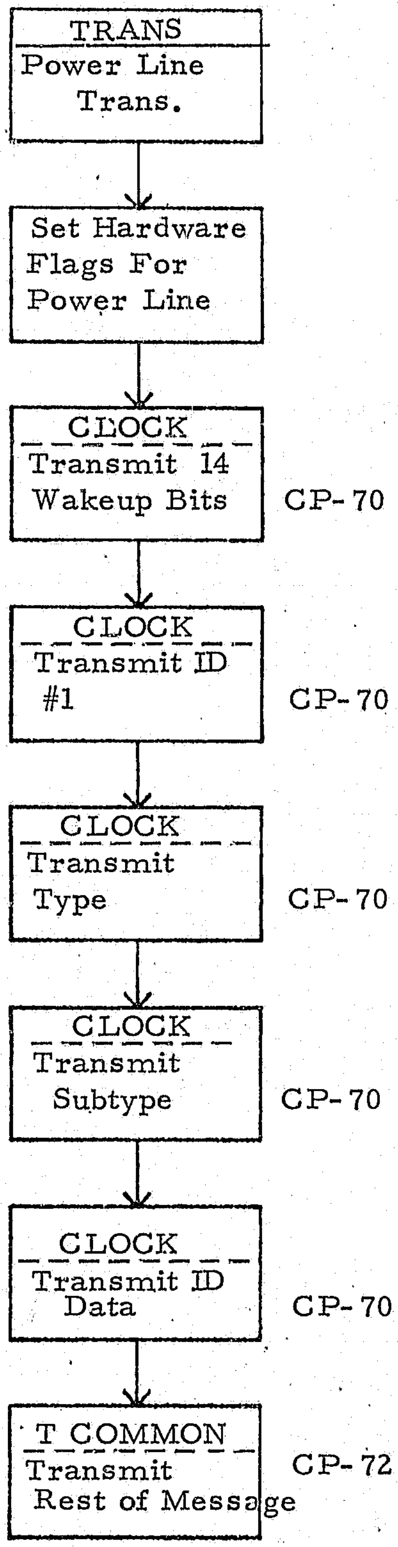

CP-65
Set Frequency (Receiver Data Ready) Flag
Store Type, Sub-Type Data Fields
Return

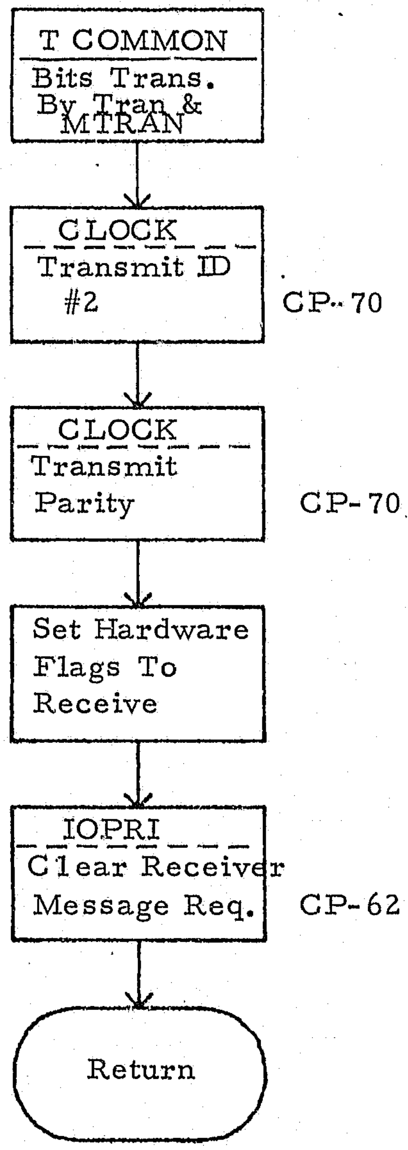

RECERR
Power Line
Receiver Error
Increment
Error Count
Is
Error Count
= 100
?
Yes
No
TIERR
Code = 86
CP-23
Return

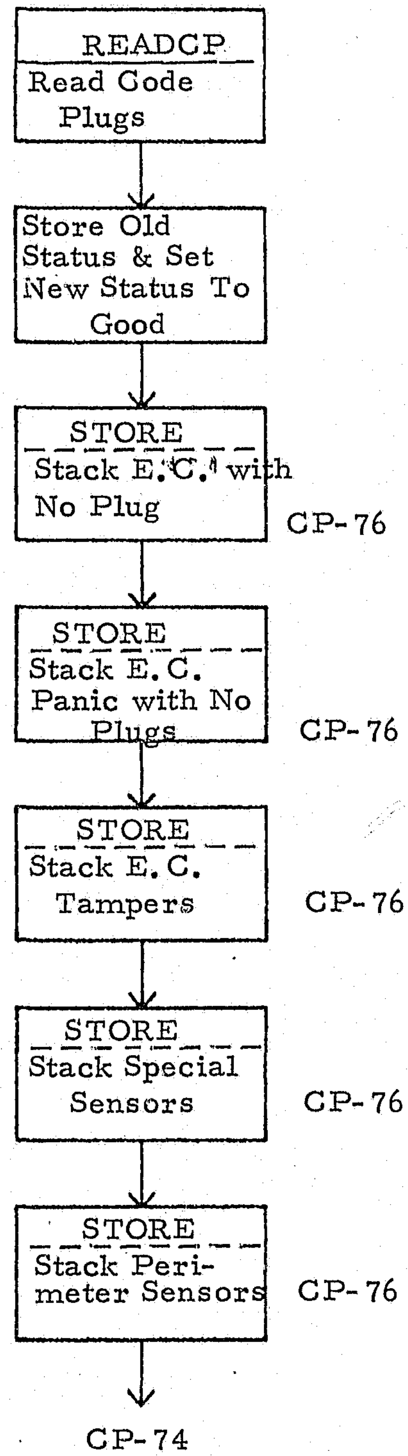

MTRANA
Transmit To Modem
Is Sensor Mode = 4 or 5 ?
No
Return
Yes
Carrier On
No
MTRAN
Modem Transmit
CP-69
Yes
Set Modem Transmit Flag (FMTR)
Return

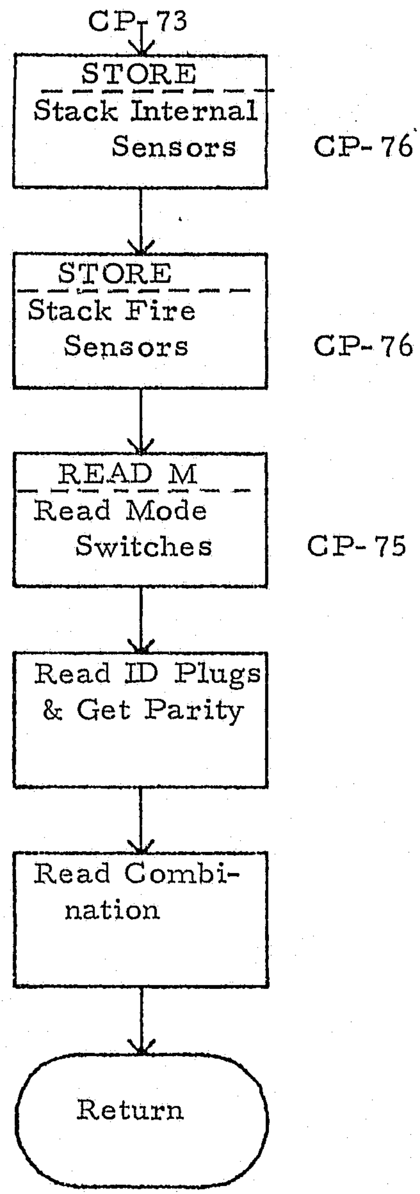

MTRAN
Modem Transmition
Reset FMTR
Set End-of-Moden-Tran. Flag
Set Modem Hardware Flags
Start 350 Mil Sec. Delay
CLOCK
Transmit ID #1
CP-70
CLOCK
Transmit ID #1
CP-70
T COMMON
Transmit Rest Of Message
CP-72

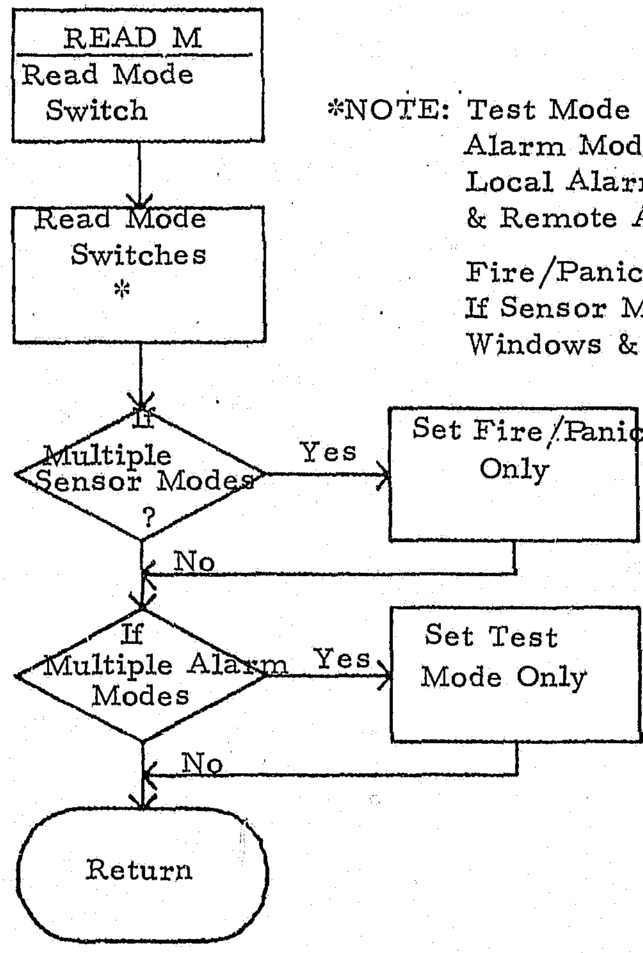

CLOCK
Transmit N Bits
If Clock Leading Edge ?
No
Yes
Output High Bit & Shift Left
N = N - 1
If N = 0 ?
No
Yes
Return


TRANS
Power Line Trans.
Set Hardware Flags For Power Line
CLOCK
Transmit 14 Wakeup Bits
CP-70
CLOCK
Transmit ID #1
CP-70
CLOCK
Transmit Type
CP-70
CLOCK
Transmit Subtype
CP-70
CLOCK
Transmit ID Data
CP-70
T COMMON
Transmit Rest of Message
CP-72


T COMMON
Bits Trans. By Tran & MTRAN
CLOCK
Transmit ID #2
CP-70
CLOCK
Transmit Parity
CP-70
Set Hardware Flags To Receive
IOPRI
Clear Receiver Message Req.
CP-62
Return


READCP
Read Code Plugs
Store Old Status & Set New Status To Good
STORE
Stack E.C. with No Plug
CP-76
STORE
Stack E.C. Panic with No Plugs
CP-76
STORE
Stack E.C. Tampers
CP-76
STORE
Stack Special Sensors
CP-76
STORE
Stack Perimeter Sensors
CP-76
CP-74


CP-73
STORE
Stack Internal Sensors
CP-76
STORE
Stack Fire Sensors
CP-76
READ M
Read Mode Switches
CP-75
Read ID Plugs & Get Parity
Read Combination
Return

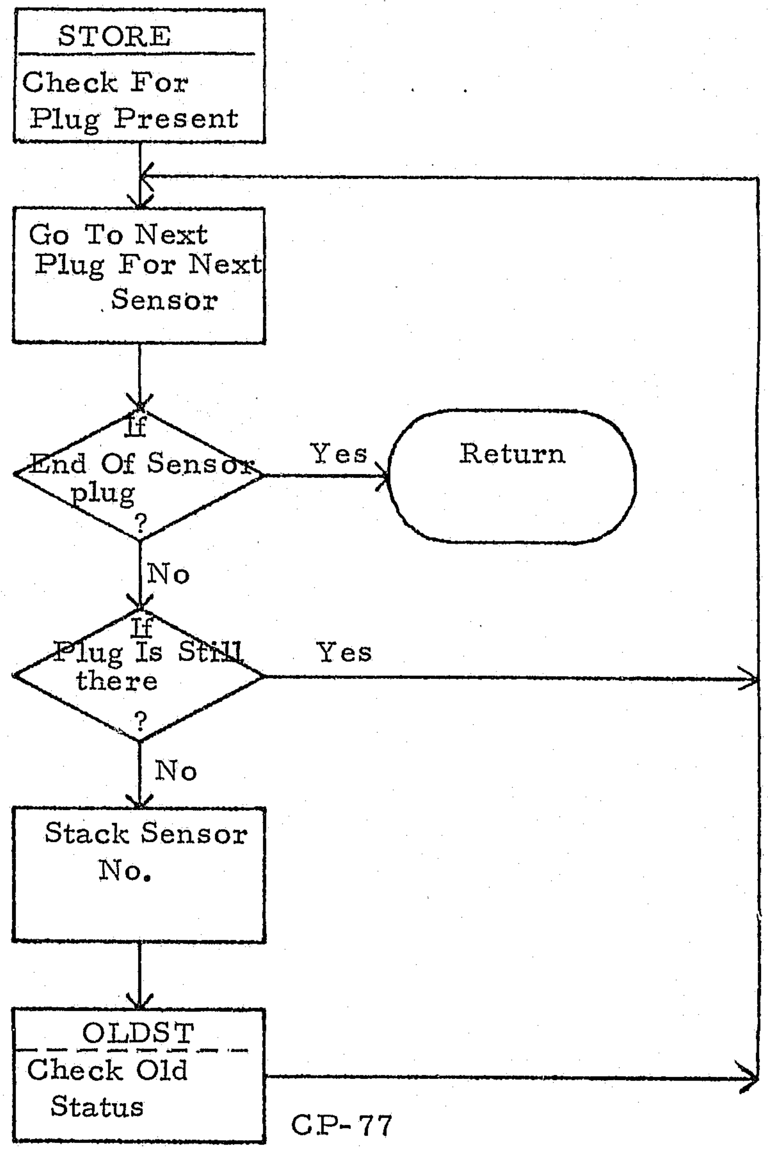


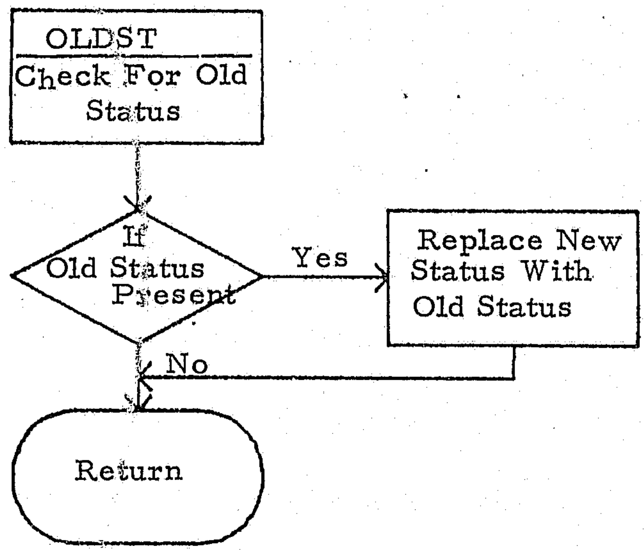
*NOTE: Test Mode Assumed If Alarm Modes Local Alert, Local Alarm, Loc/Remote, & Remote Are Not Set.

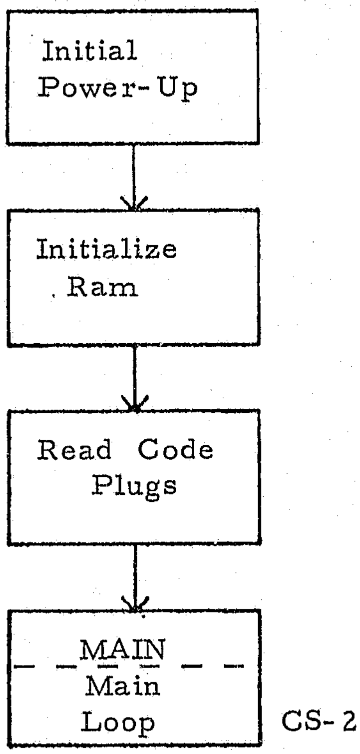
Fire/Panic Mode Assumed If Sensor Modes Doors/ Windows & All Are Not Set

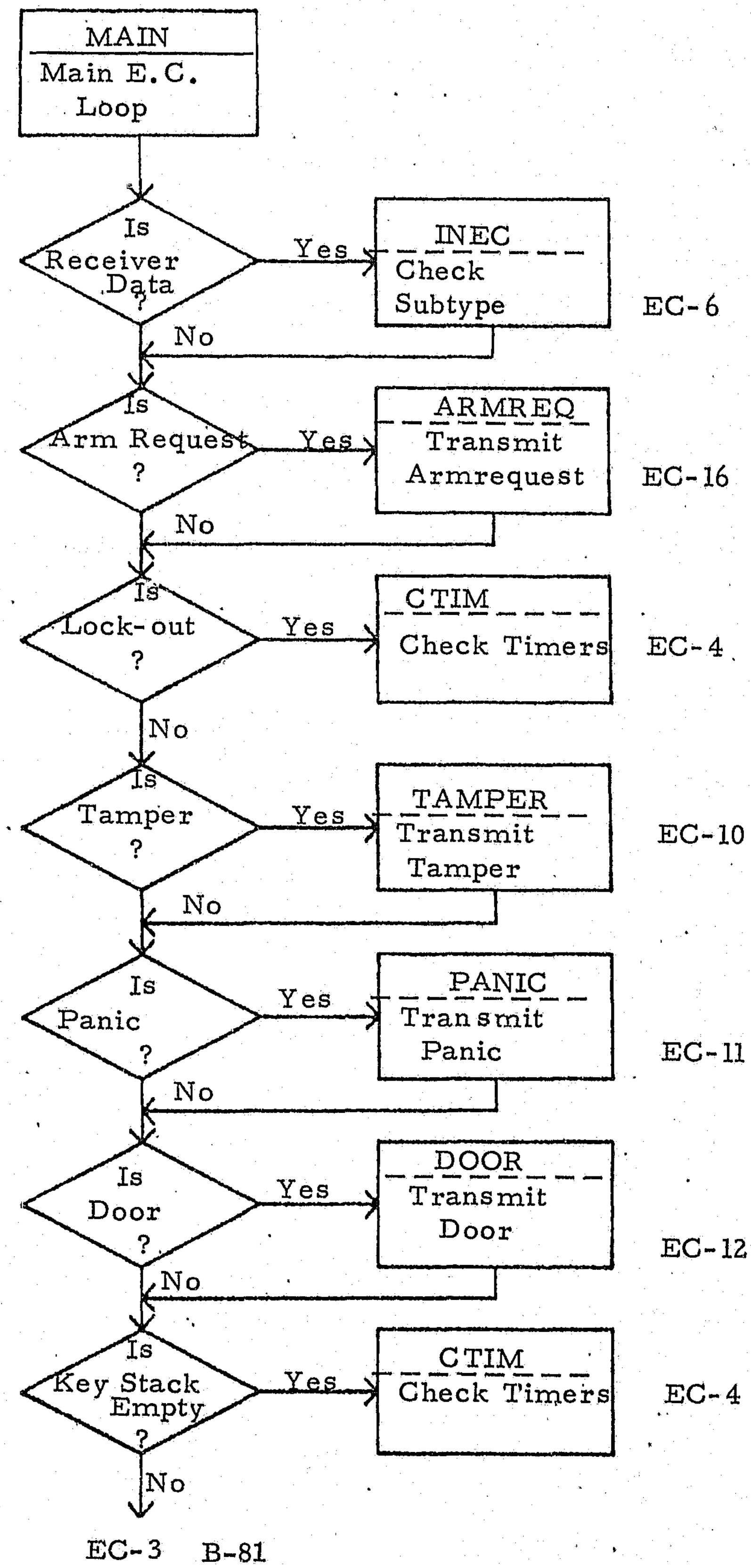
CONTINUED

4 OF 5

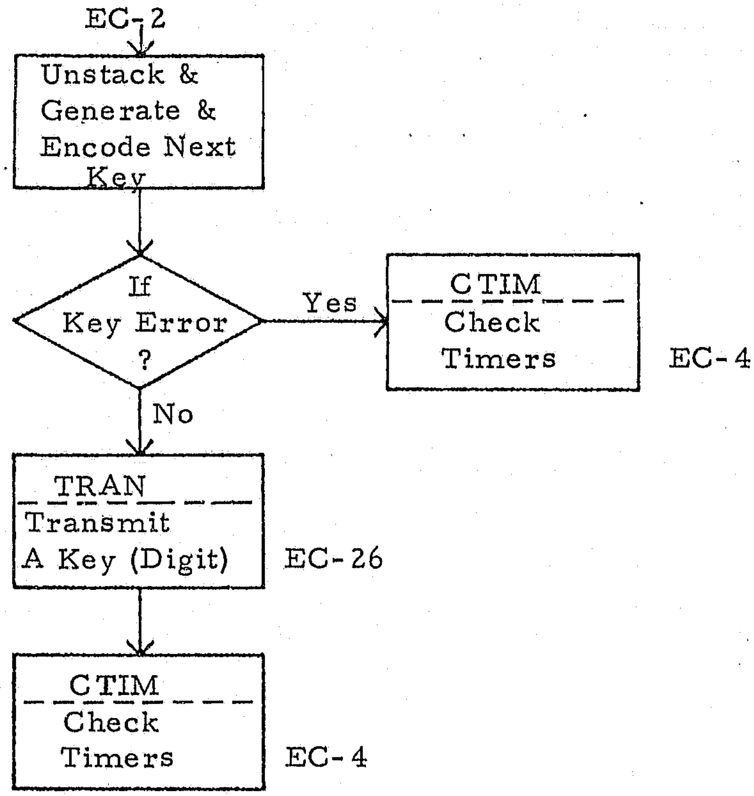

STORE
Check For Plug Present
Go To Next Plug For Next Sensor
If End Of Sensor plug ?
Yes
Return
No
If Plug Is Still there ?
Yes
No
Stack Sensor No.
OLDST
Check Old Status
CP-77

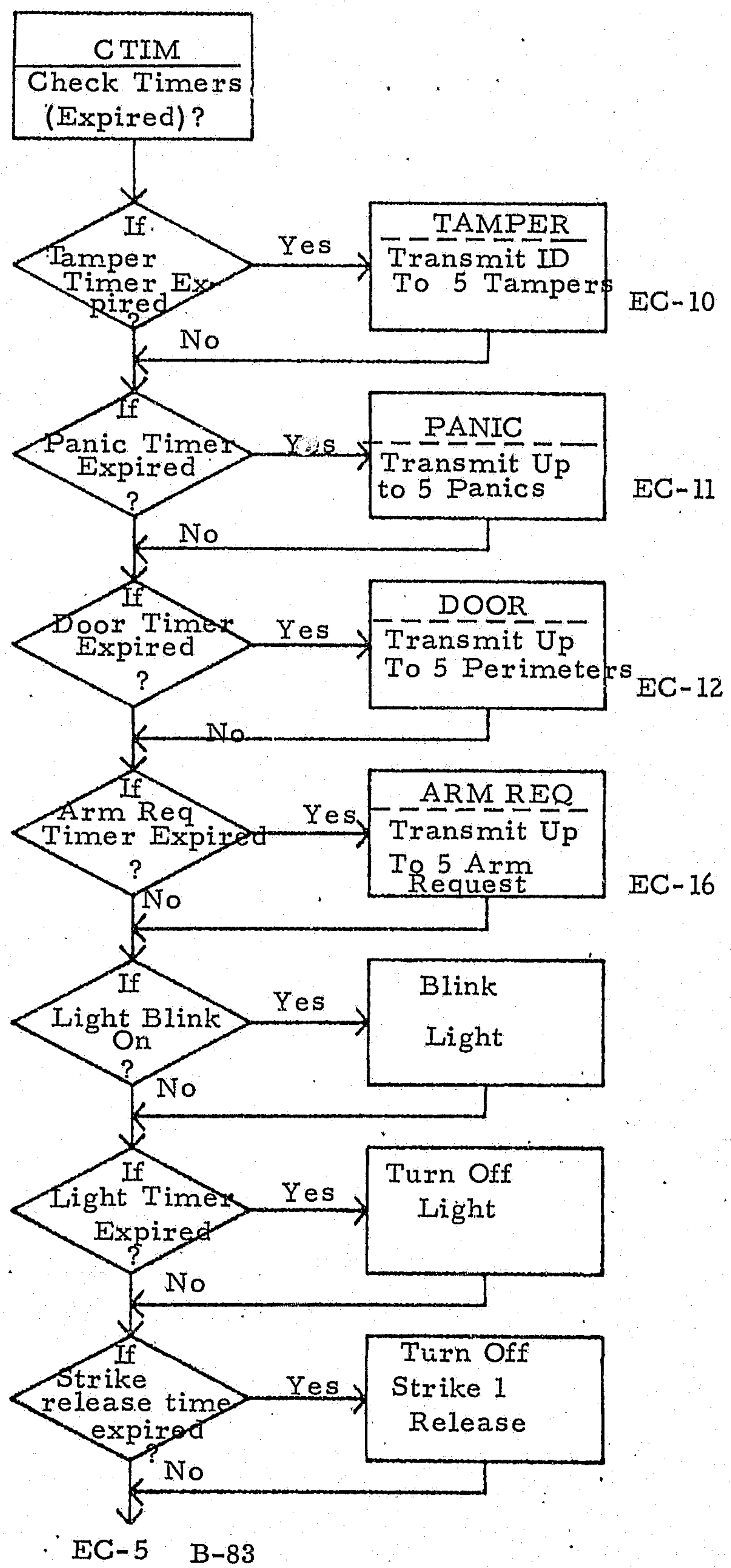

OLDST
Check For Old Status
If Old Status Present
Yes
Replace New Status With Old Status
No
Return

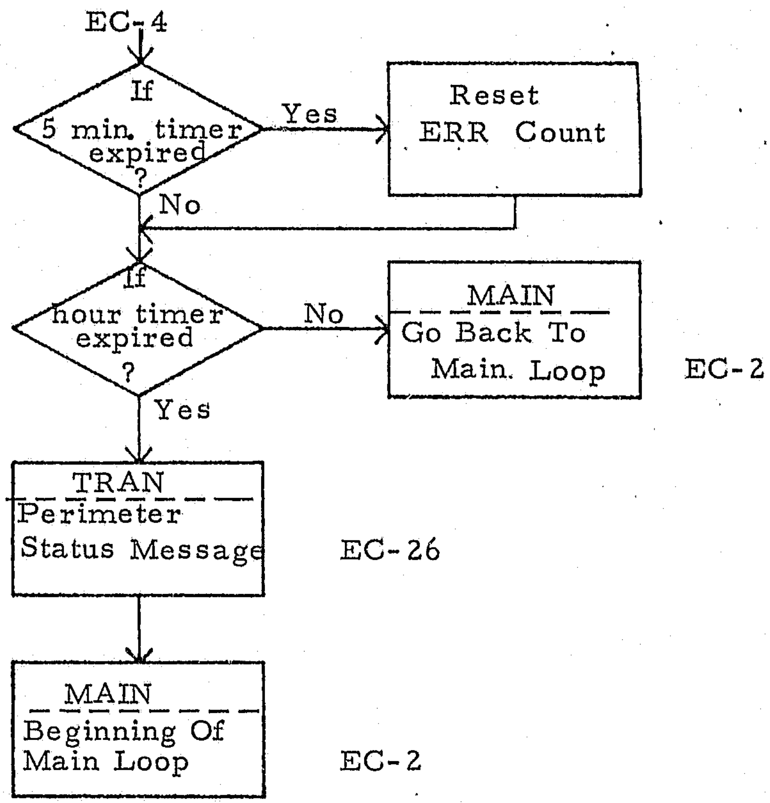

Initial Power-Up
Initialize Ram
Read Code Plugs
MAIN
Main Loop
CS-2



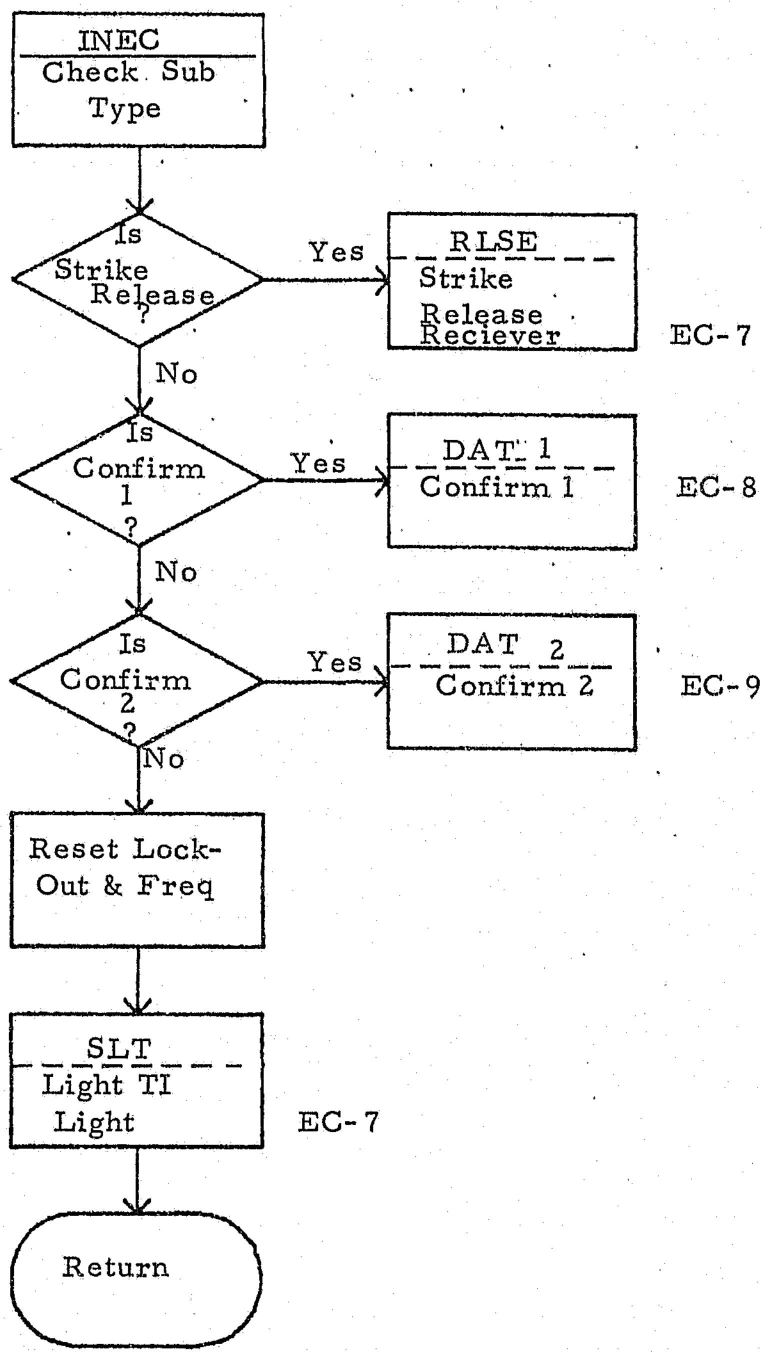
MAIN
Main E.C. Loop
Is Receiver Data ?
Yes
INEC
Check Subtype
EC-6
No
Is Arm Request ?
Yes
ARMREQ
Transmit Armrequest
EC-16
No
Is Lock-out ?
Yes
CTIM
Check Timers
EC-4
No
Is Tamper ?
Yes
TAMPER
Transmit Tamper
EC-10
No
Is Panic ?
Yes
PANIC
Transmit Panic
EC-11
No
Is Door ?
Yes
DOOR
Transmit Door
EC-12
No
Is Key Stack Empty ?
Yes
CTIM
Check Timers
EC-4
No
EC-3

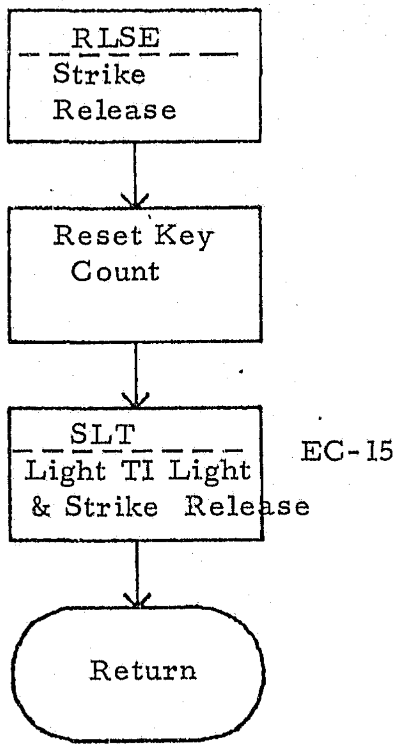

EC-2
Unstack & Generate & Encode Next Key
If Key Error ?
Yes
CTIM
Check Timers
EC-4
No
TRAN
Transmit A Key (Digit)
EC-26
CTIM
Check Timers
EC-4

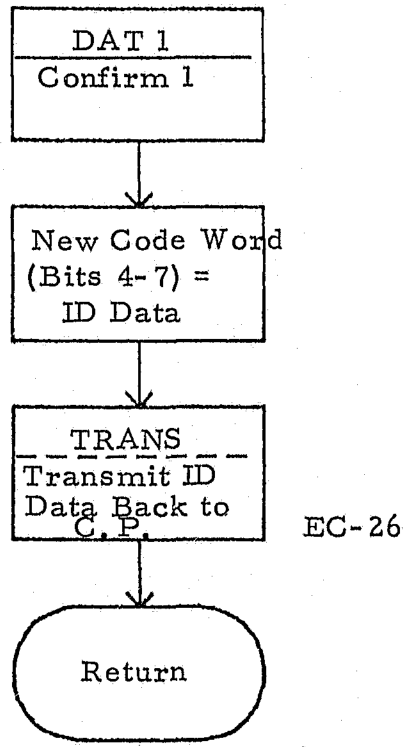

CTIM
Check Timers (Expired)?
If Tamper Timer Expired?
Yes
TAMPER
Transmit ID To 5 Tampers
EC-10
No
If Panic Timer Expired?
Yes
PANIC
Transmit Up to 5 Panics
EC-11
No
If Door Timer Expired?
Yes
DOOR
Transmit Up To 5 Perimeters
EC-12
No
If Arm Req Timer Expired?
Yes
ARM REQ
Transmit Up To 5 Arm Request
EC-16
No
If Light Blink On?
Yes
Blink Light
No
If Light Timer Expired?
Yes
Turn Off Light
No
If Strike release time expired?
Yes
Turn Off Strike 1 Release
No
EC-5

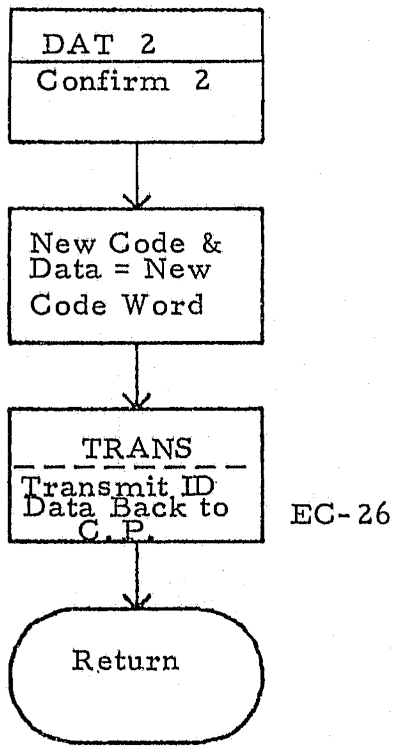


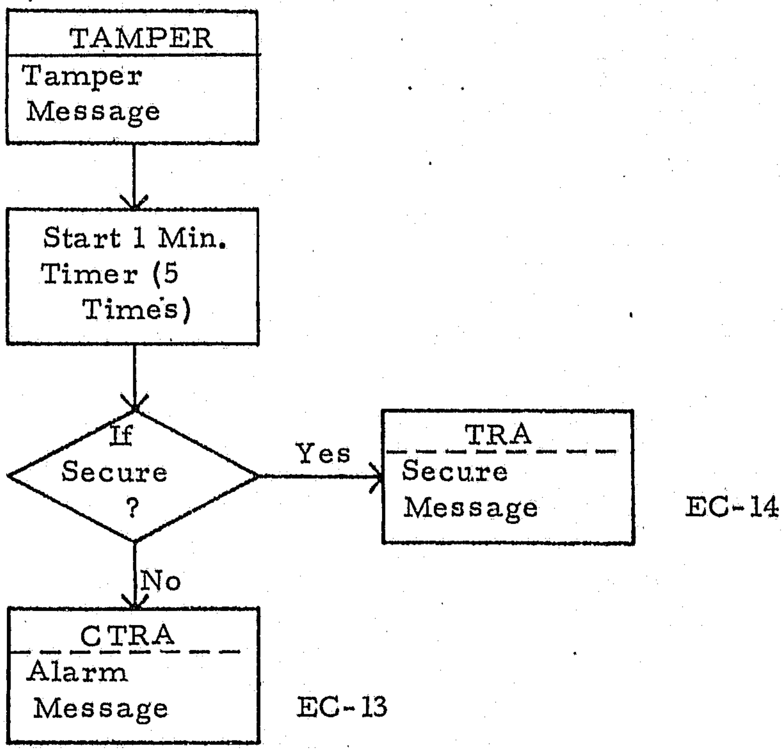
EC-4
If
5 min. timer
expired
?
Yes
Reset
ERR Count
No
If
hour timer
expired
?
No
MAIN
Go Back To
Main. Loop
EC-2
Yes
TRAN
Perimeter
Status Message
EC-26
MAIN
Beginning Of
Main Loop
EC-2

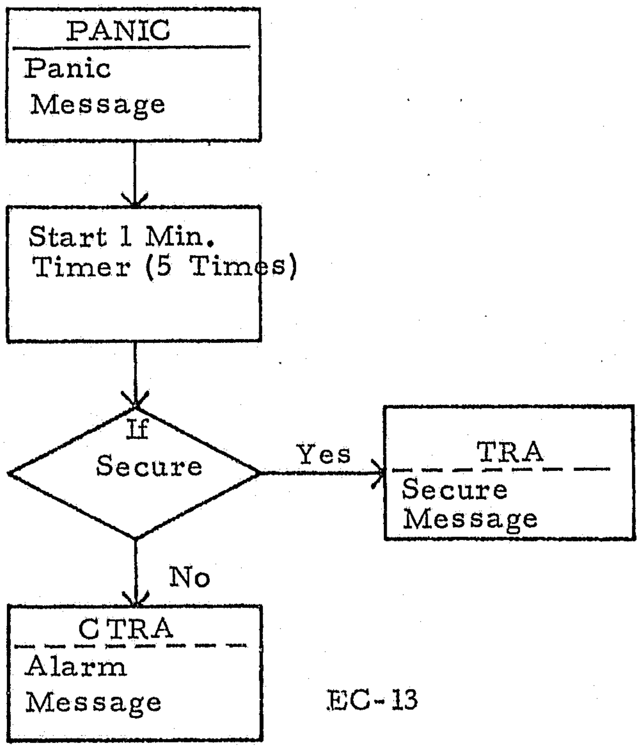

INEC
Check Sub Type
Is Strike Release ?
Yes
RLSE
Strike Release Reciever
EC-7
No
Is Confirm 1 ?
Yes
DAT 1
Confirm 1
EC-8
No
Is Confirm 2 ?
Yes
DAT 2
Confirm 2
EC-9
No
Reset Lock-Out & Freq
SLT
Light TI Light
EC-7
Return


RLSE
Strike Release
Reset Key Count
SLT
Light TI Light & Strike Release
EC-15
Return


DAT 1
Confirm 1
New Code Word
(Bits 4-7) =
ID Data
TRANS
Transmit ID
Data Back to
C. P.
EC-26
Return

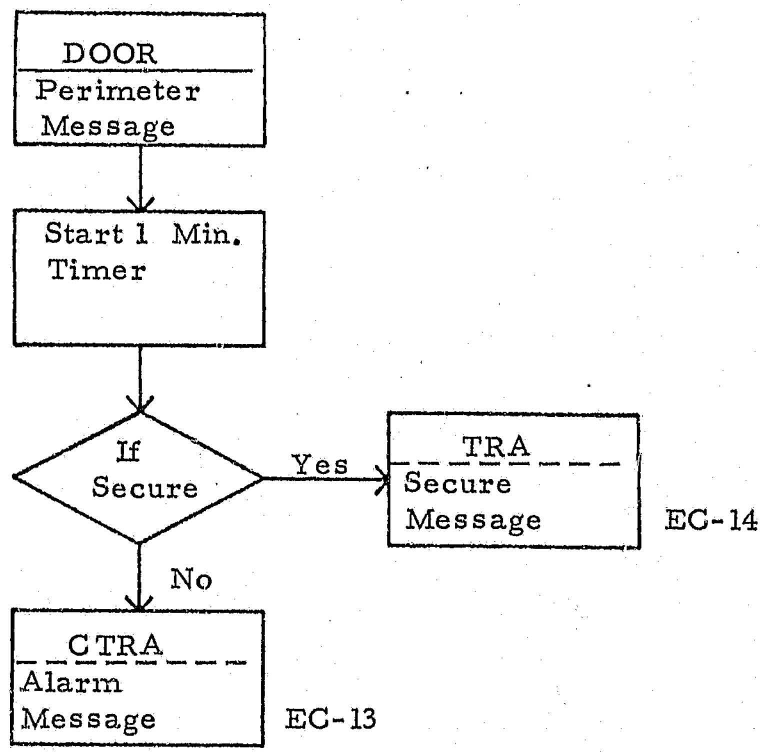

DAT 2
Confirm 2
New Code & Data = New Code Word
TRANS
Transmit ID Data Back to C.P.
EC-26
Return

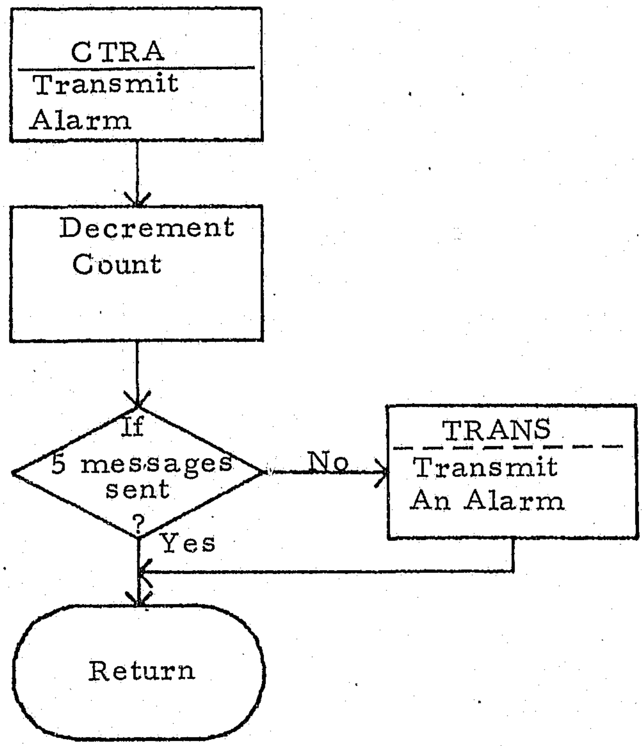

TAMPER
Tamper Message
Start 1 Min. Timer (5 Times)
If Secure ?
Yes
TRA
Secure Message
EC-14
No
CTRA
Alarm Message
EC-13


PANIC
Panic
Message
Start 1 Min.
Timer (5 Times)
If
Secure
Yes
TRA
Secure
Message
No
C TRA
Alarm
Message

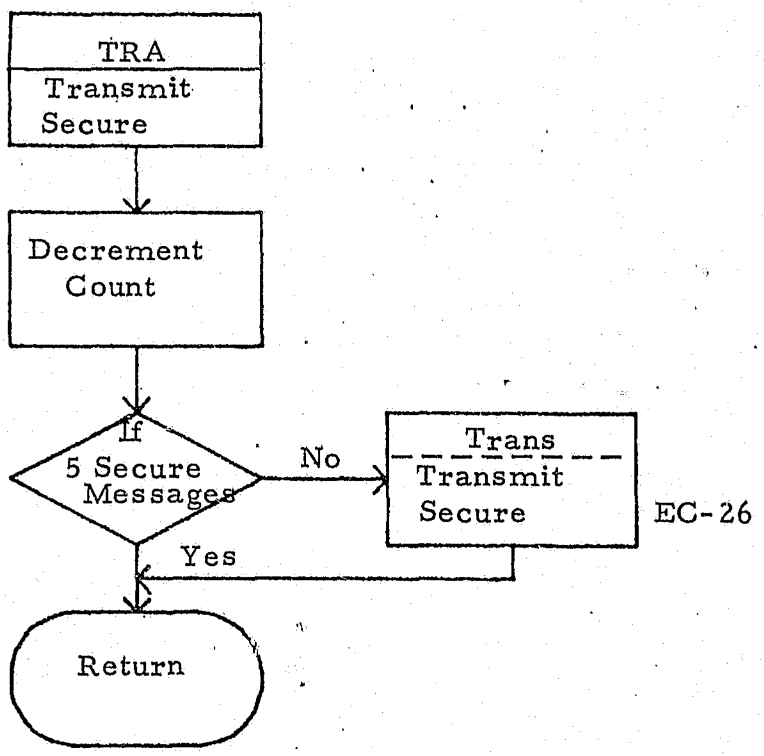
EC-14

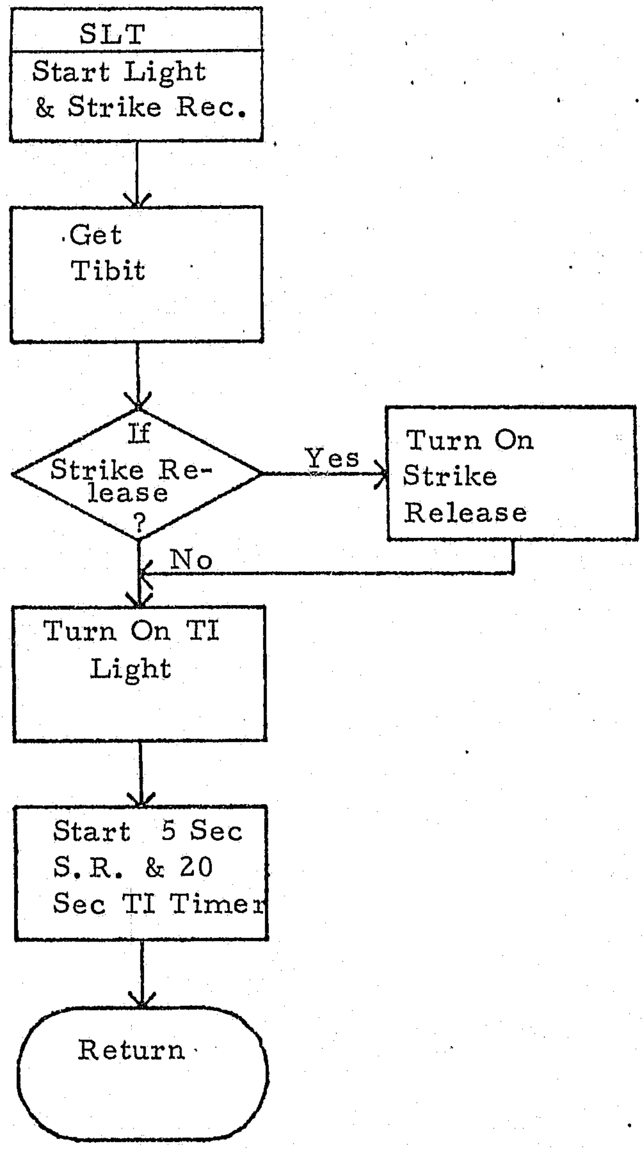
EC-13

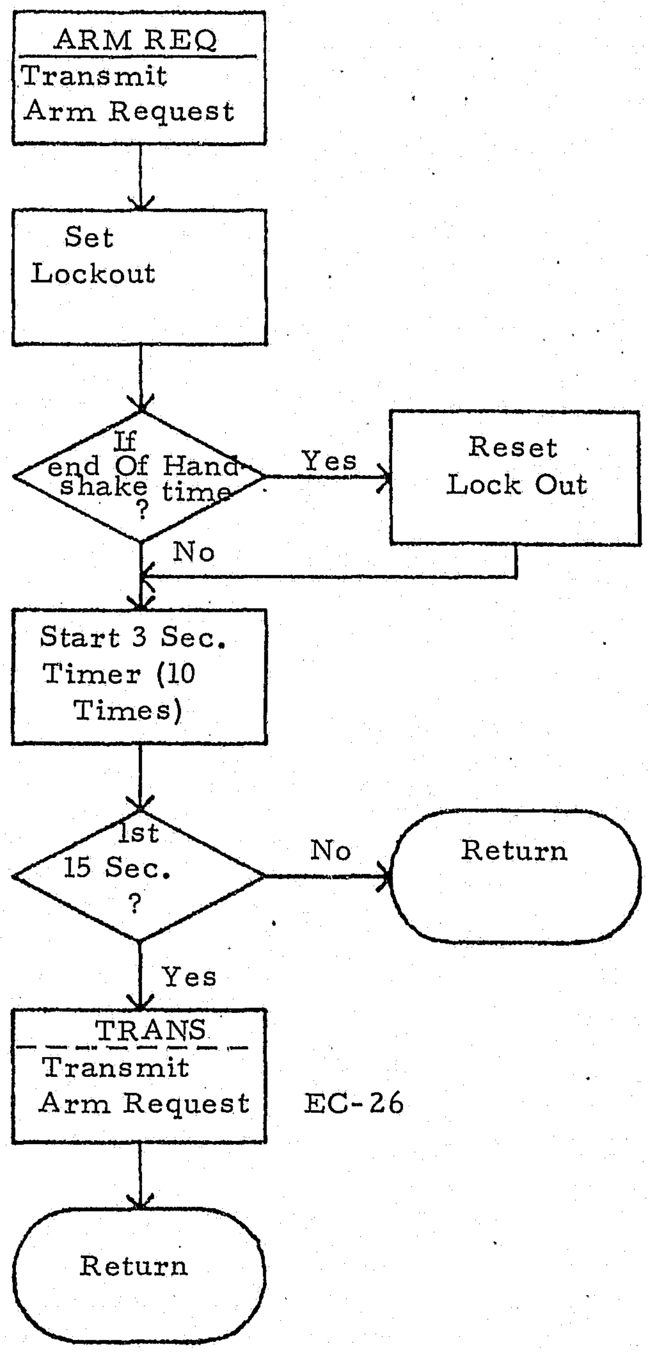

DOOR
Perimeter Message
Start 1 Min. Timer
If Secure
Yes
TRA
Secure Message
EC-14
No
CTRA
Alarm Message
EC-13

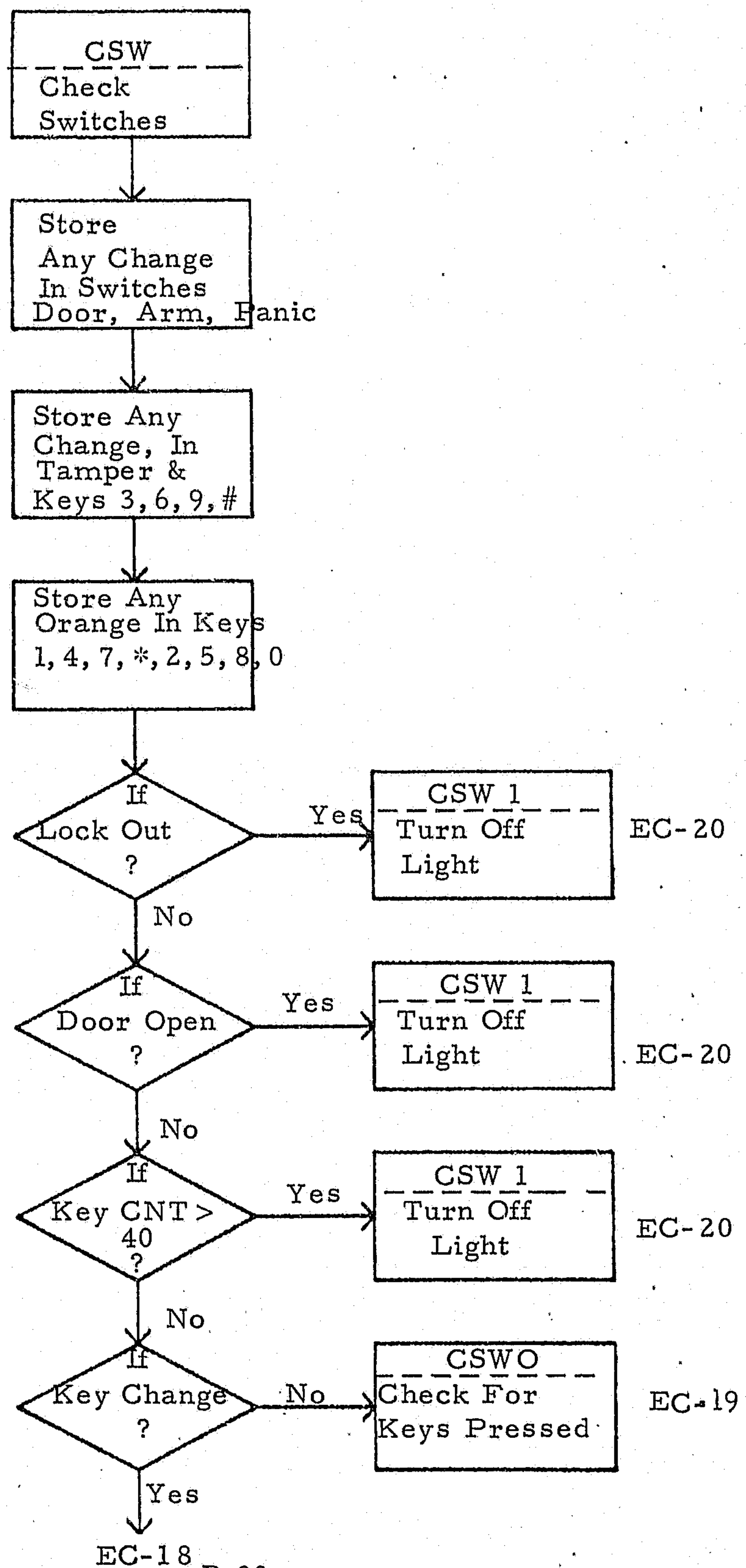

CTRA
Transmit
Alarm
Decrement
Count
If
5 messages
sent
?
No
Yes
TRANS
Transmit
An Alarm
Return

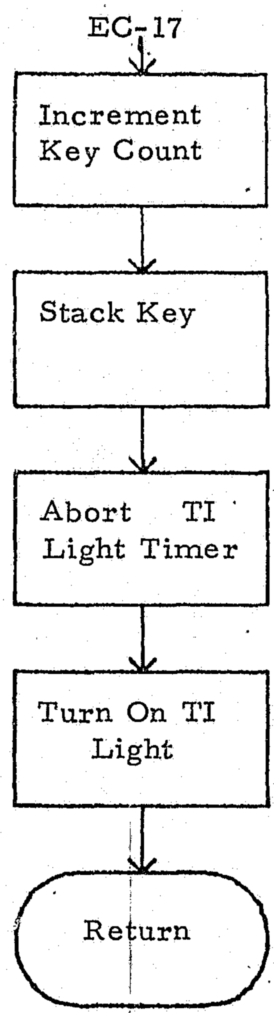
EC-26

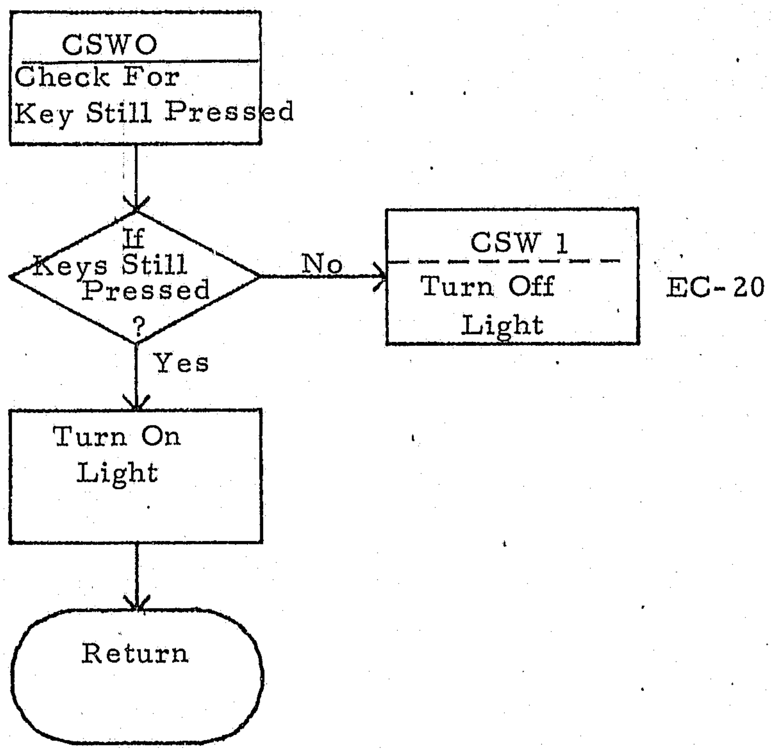

TRA
Transmit
Secure
Decrement
Count
If
5 Secure
Messages
No
Yes
Trans
Transmit
Secure
EC-26
Return

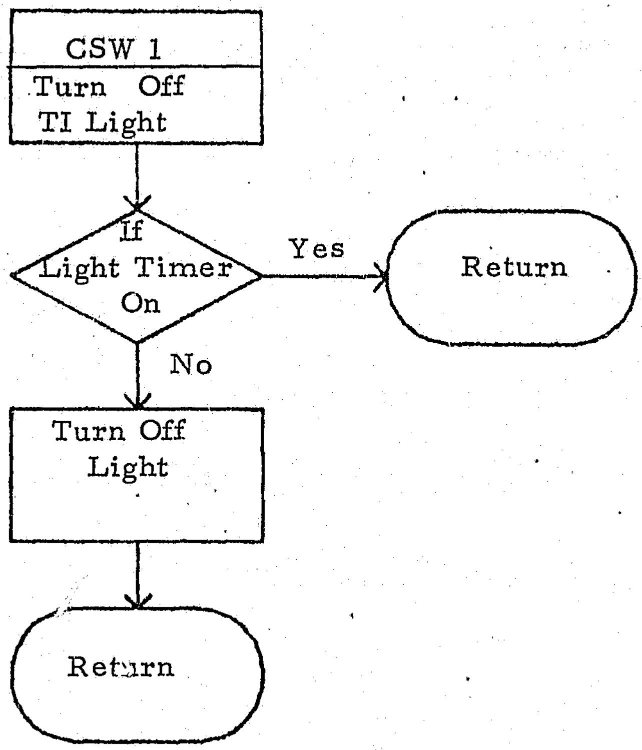

SLT
Start Light & Strike Rec.
Get Tibit
If Strike Release ?
Yes
Turn On Strike Release
No
Turn On TI Light
Start 5 Sec S.R. & 20 Sec TI Timer
Return

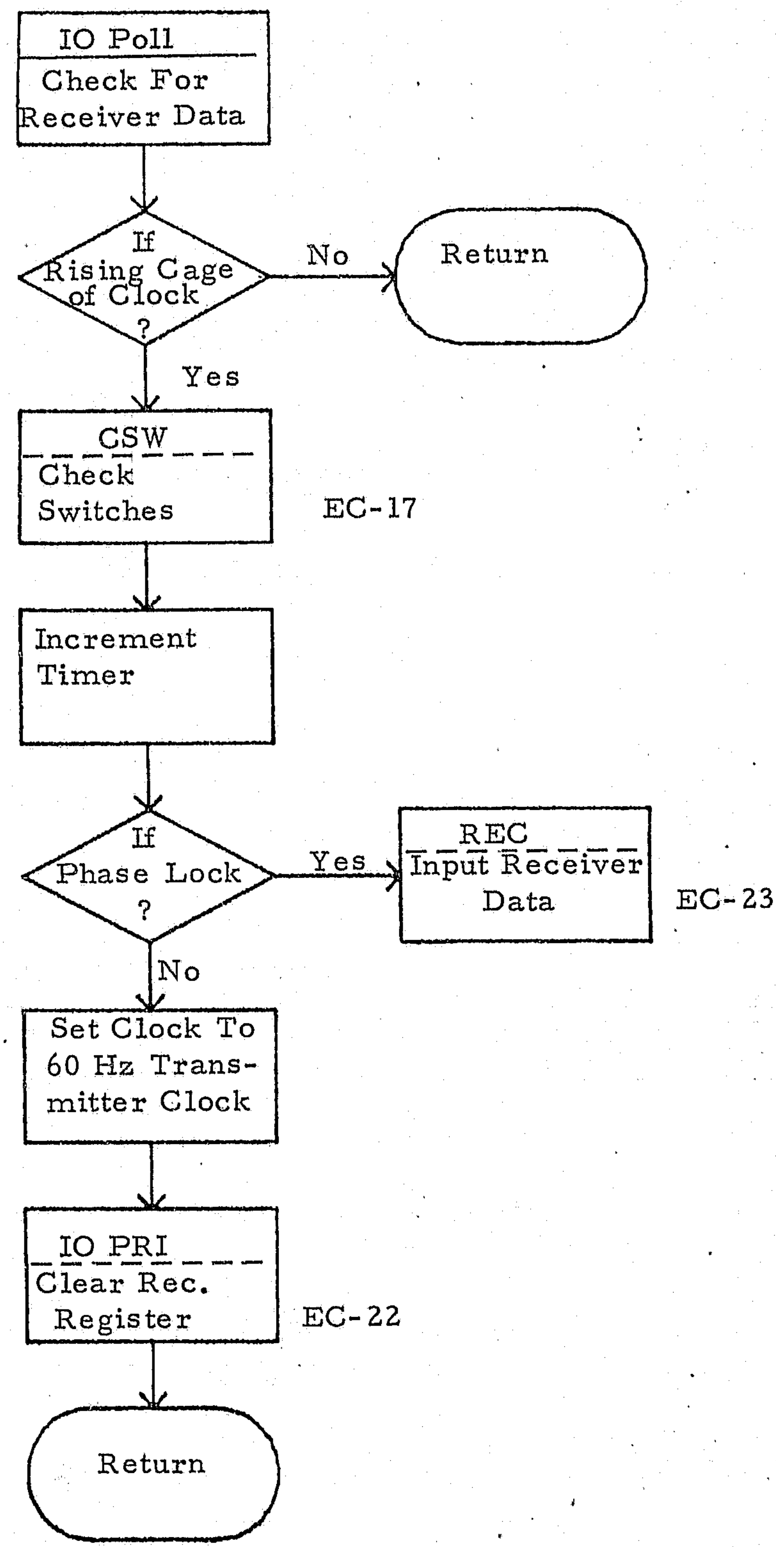

ARM REQ
Transmit Arm Request
Set Lockout
If end Of Hand shake time ?
Yes
Reset Lock Out
No
Start 3 Sec. Timer (10 Times)
1st 15 Sec. ?
No
Return
Yes
TRANS
Transmit Arm Request
EC-26
Return

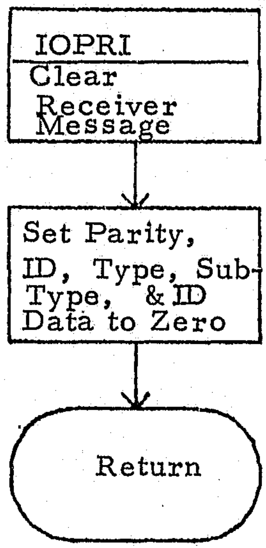

CSW
Check Switches
Store Any Change In Switches Door, Arm, Panic
Store Any Change, In Tamper & Keys 3, 6, 9, #
Store Any Orange In Keys 1, 4, 7, *, 2, 5, 8, 0
If Lock Out ?
Yes
CSW 1
Turn Off Light
EC-20
No
If Door Open ?
Yes
CSW 1
Turn Off Light
EC-20
No
If Key CNT > 40 ?
Yes
CSW 1
Turn Off Light
EC-20
No
If Key Change ?
No
CSWO
Check For Keys Pressed
EC-19
Yes
EC-18

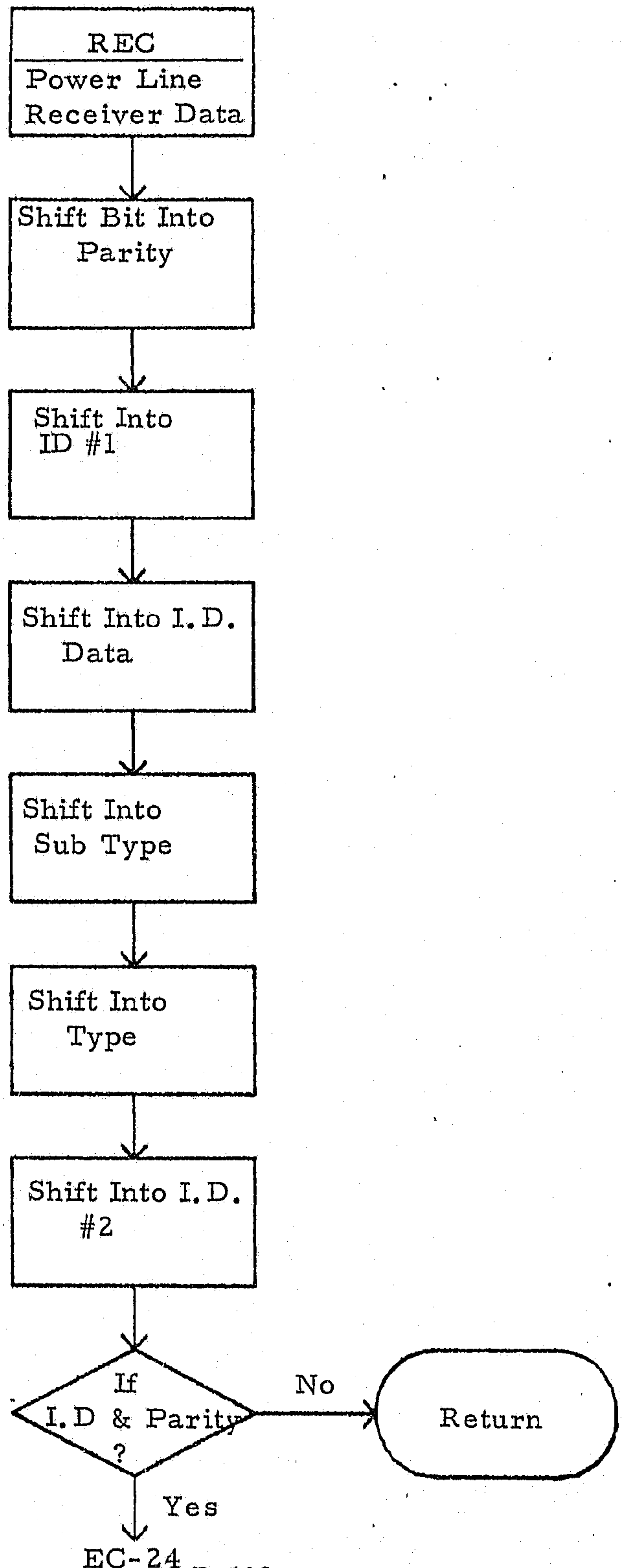

EC-17
Increment Key Count
Stack Key
Abort TI Light Timer
Turn On TI Light
Return


CSWO
Check For
Key Still Pressed
If
Keys Still
Pressed
?
No
CSW 1
Turn Off
Light
EC-20
Yes
Turn On
Light
Return

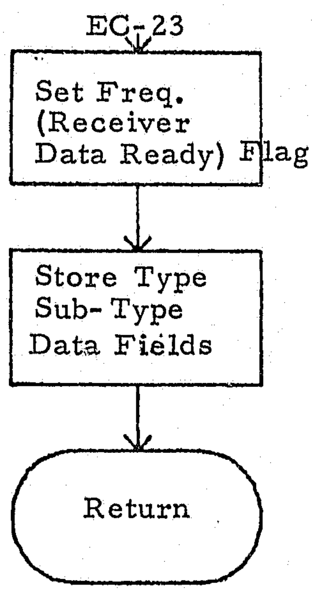

CSW 1
Turn Off
TI Light
If
Light Timer
On
Yes
Return
No
Turn Off
Light
Return

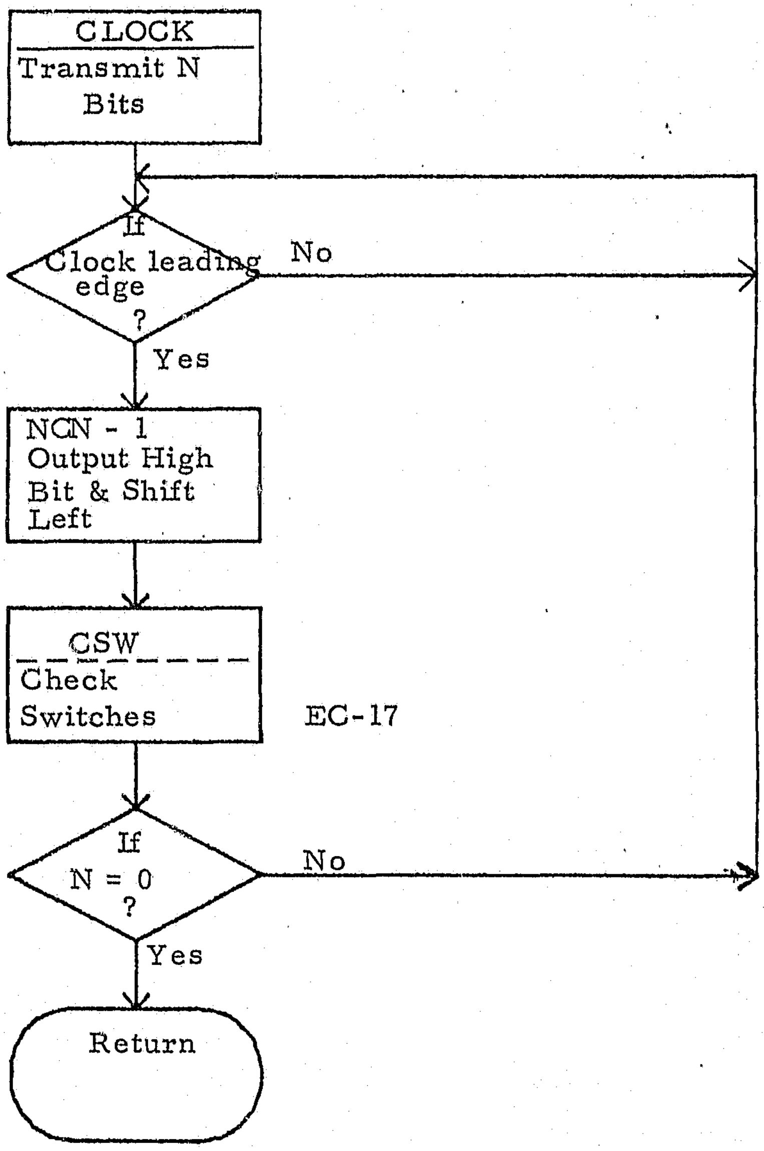

IO Poll
Check For Receiver Data
If Rising Cage of Clock ?
No
Return
Yes
CSW
Check Switches
EC-17
Increment Timer
If Phase Lock ?
Yes
REC
Input Receiver Data
EC-23
No
Set Clock To 60 Hz Transmitter Clock
IO PRI
Clear Rec. Register
EC-22
Return

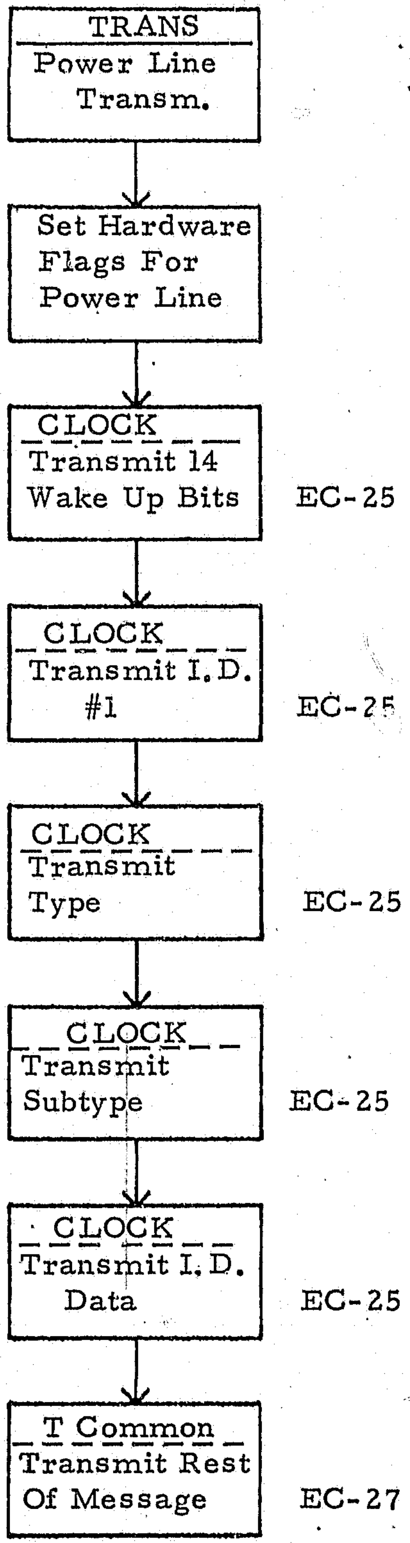

IOPRI
Clear Receiver Message
Set Parity, ID, Type, Sub-Type, & ID Data to Zero
Return

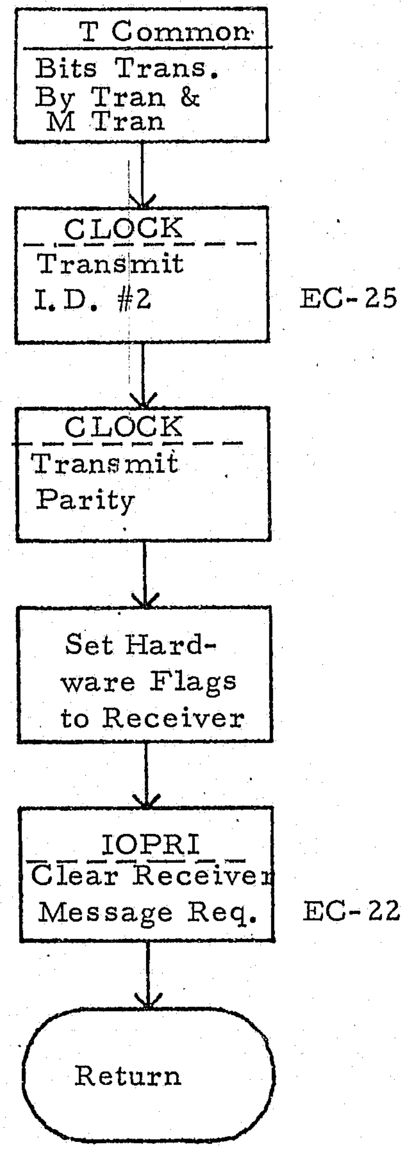

REC
Power Line
Receiver Data
Shift Bit Into
Parity
Shift Into
ID #1
Shift Into I.D.
Data
Shift Into
Sub Type
Shift Into
Type
Shift Into I.D.
#2
If
I.D & Parity
?
No
Return
Yes
EC-24

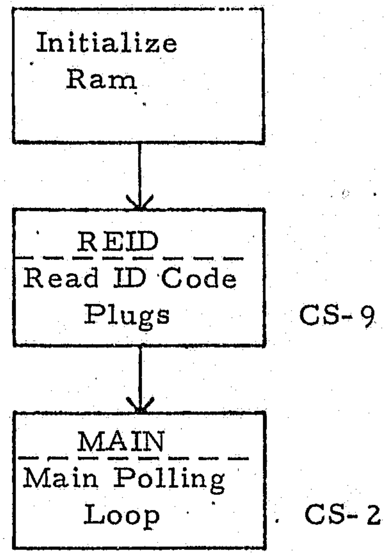
B-102

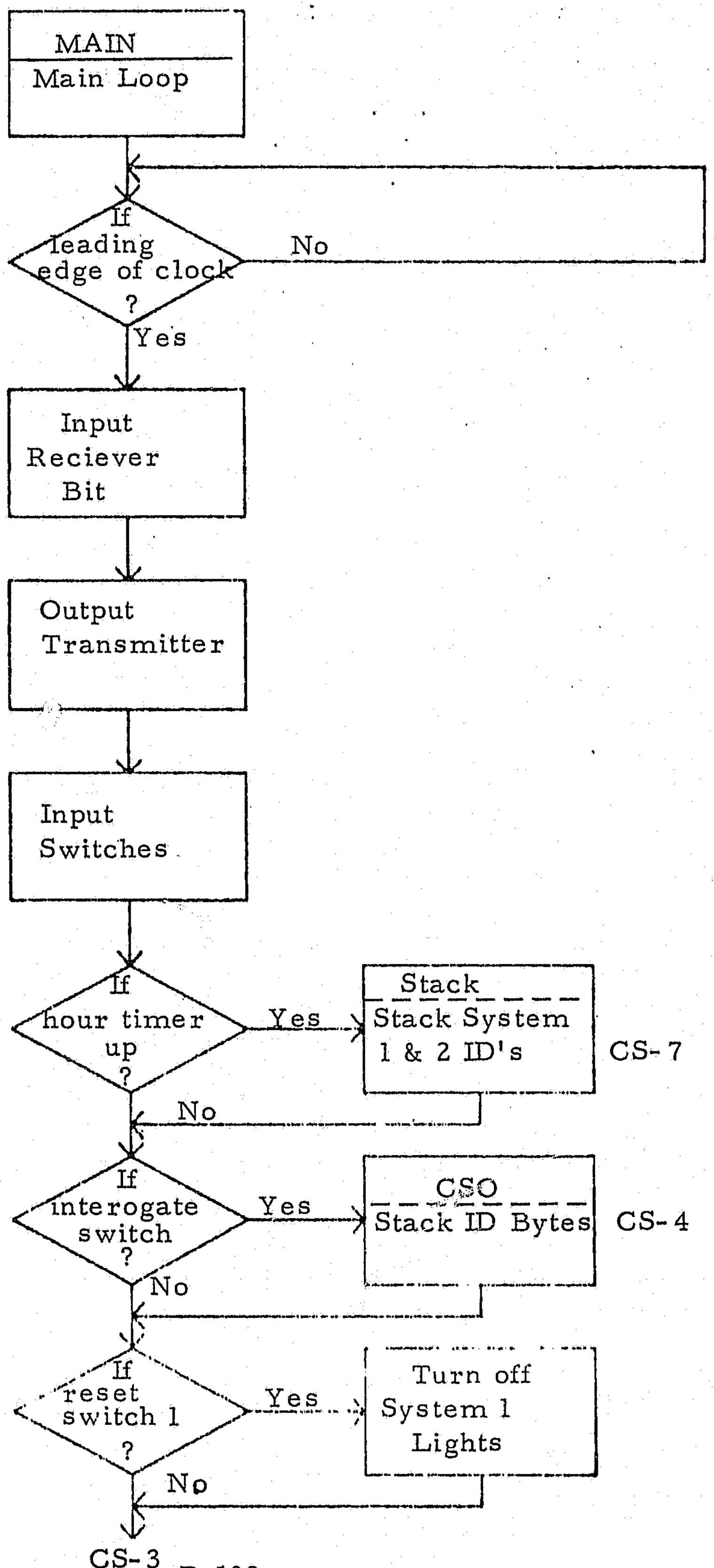

EC-23
Set Freq.
(Receiver
Data Ready) Flag
Store Type
Sub-Type
Data Fields
Return

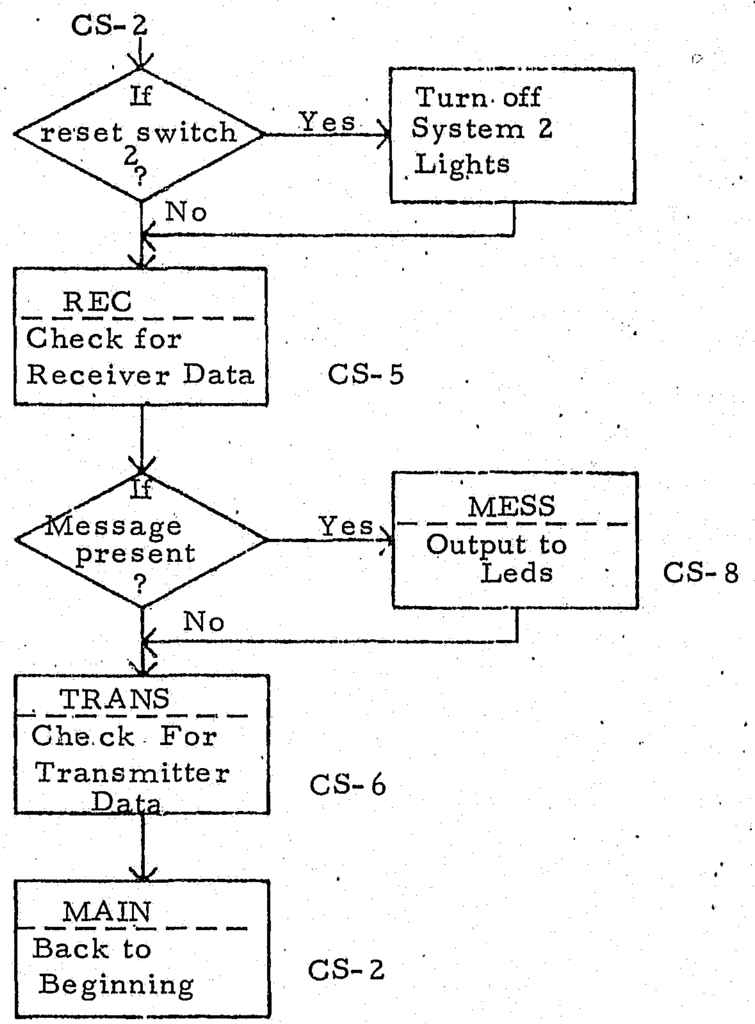

CLOCK
Transmit N Bits
If Clock leading edge ?
No
Yes
NCN - 1
Output High Bit & Shift Left
CSW
Check Switches
EC-17
If N = 0 ?
No
Yes
Return

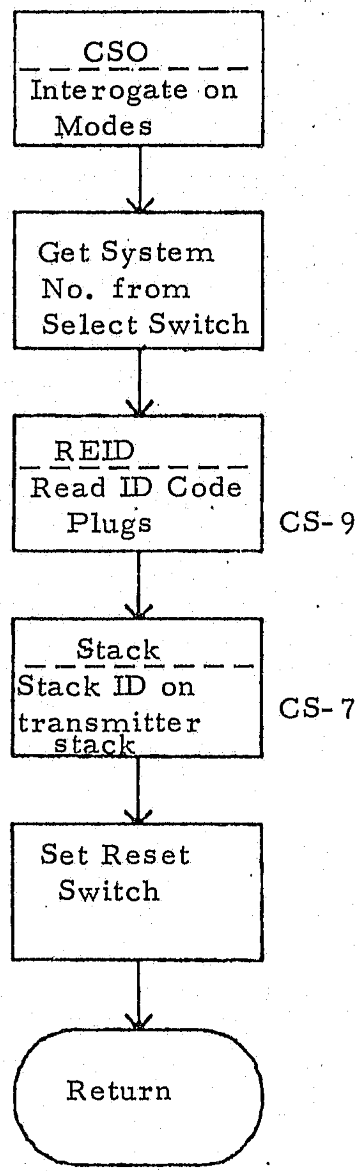

TRANS
Power Line Transm.
Set Hardware Flags For Power Line
CLOCK
Transmit 14 Wake Up Bits
EC-25
CLOCK
Transmit I.D. #1
EC-25
CLOCK
Transmit Type
EC-25
CLOCK
Transmit Subtype
EC-25
CLOCK
Transmit I.D. Data
EC-25
T Common
Transmit Rest Of Message
EC-27

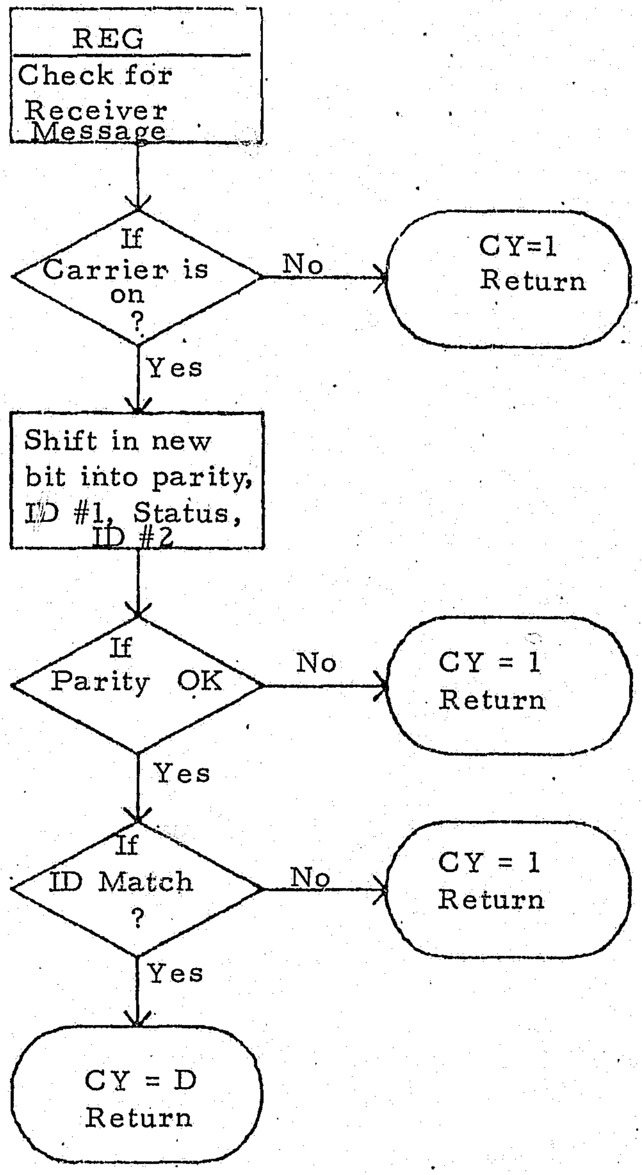

T Common
Bits Trans.
By Tran &
M Tran
CLOCK
Transmit
I.D. #2
EC-25
CLOCK
Transmit
Parity
Set Hard-
ware Flags
to Receiver
IOPRI
Clear Receiver
Message Req.
EC-22
Return

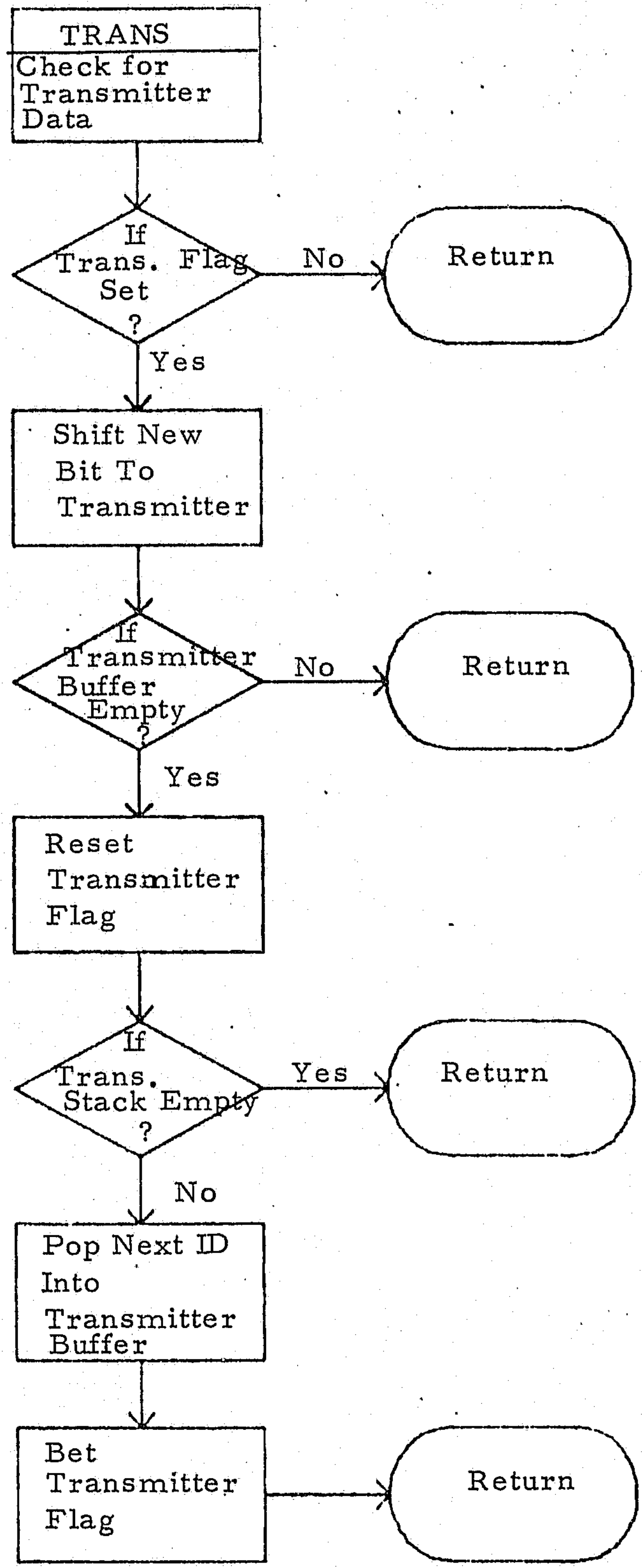

Initialize
Ram
REID
Read ID Code
Plugs
CS-9
MAIN
Main Polling
Loop
CS-2

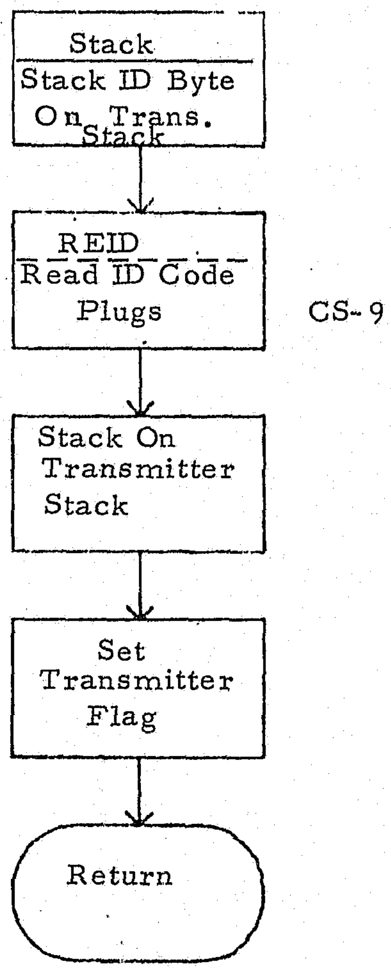

MAIN
Main Loop
If leading edge of clock ?
No
Yes
Input Reciever Bit
Output Transmitter
Input Switches
If hour timer up ?
Yes
Stack
Stack System 1 & 2 ID's
CS-7
No
If interogate switch ?
Yes
CSO
Stack ID Bytes
CS-4
No
If reset switch 1 ?
Yes
Turn off System 1 Lights
No
CS-3

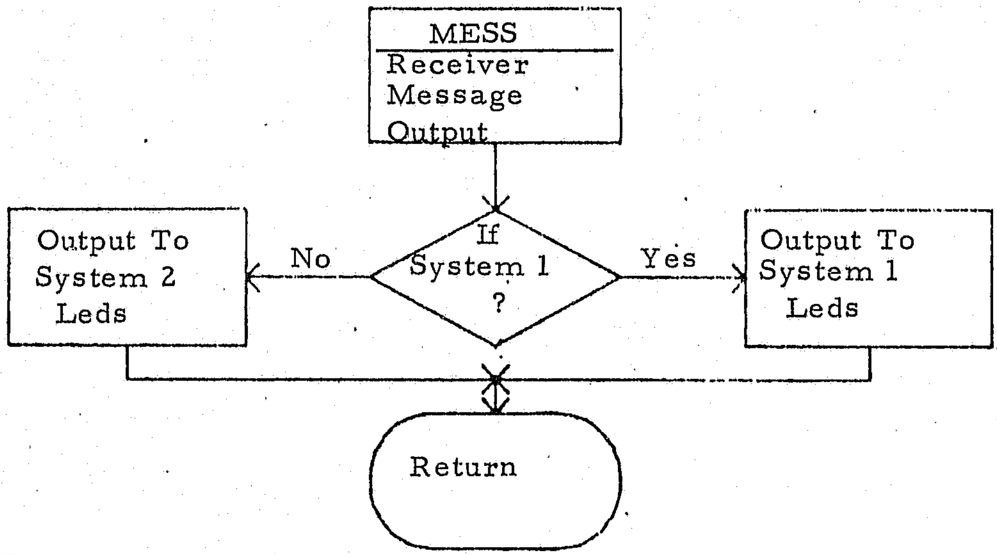

CS-2
If reset switch 2 ?
Yes
Turn off System 2 Lights
No
REC
Check for Receiver Data
CS-5
If Message present ?
Yes
MESS
Output to Leds
CS-8
No
TRANS
Check For Transmitter Data
CS-6
MAIN
Back to Beginning
CS-2

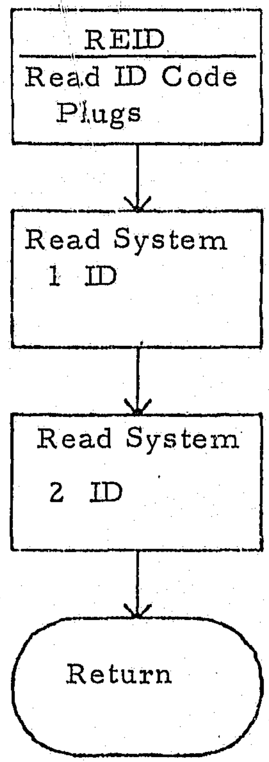

CSO
Interogate on Modes
Get System No. from Select Switch
REID
Read ID Code Plugs
CS-9
Stack
Stack ID on transmitter stack
CS-7
Set Reset Switch
Return


REG
Check for Receiver Message
If Carrier is on ?
No
CY=1 Return
Yes
Shift in new bit into parity, ID #1, Status, ID #2
If Parity OK
No
CY = 1 Return
Yes
If ID Match ?
No
CY = 1 Return
Yes
CY = D Return


TRANS
Check for Transmitter Data
If Trans. Flag Set ?
No
Return
Yes
Shift New Bit To Transmitter
If Transmitter Buffer Empty ?
No
Return
Yes
Reset Transmitter Flag
If Trans. Stack Empty ?
Yes
Return
No
Pop Next ID Into Transmitter Buffer
Bet Transmitter Flag
Return


Stack
Stack ID Byte
On Trans. Stack
REID
Read ID Code Plugs
CS-9
Stack On Transmitter Stack
Set Transmitter Flag
Return


MESS
Receiver
Message
Output
If
System 1
?
No
Yes
Output To
System 2
Leds
Output To
System 1
Leds
Return


REID
Read ID Code Plugs
Read System 1 ID
Read System 2 ID
Return

Appendix C

BAS SOFTWARE PROGRAM LISTING

TROUBLE INDICATOR ERROR CODES

```
00 - NO TROUBLE
------------SENSORS-------------
          TYPE                    LOCATION
01 - * EXTERNAL SENSOR # 1---------.........................
02 - * EXTERNAL SENSOR # 2---------.........................
03 - * EXTERNAL SENSOR # 3---------.........................
04 - * EXTERNAL SENSOR # 4---------.........................
13 - * ENTRANCE CONTROL # 1 DOOR---.........................
14 - * ENTRANCE CONTROL # 2 DOOR---.........................
17 - * INTERNAL SENSOR # 1---------.........................
18 - * INTERNAL SENSOR # 2---------.........................
19 - * INTERNAL SENSOR # 3---------.........................
20 - * INTERNAL SENSOR # 4---------.........................
33 - * FIRE SENSOR # 1-------------.........................
34 - * FIRE SENSOR # 2-------------.........................
35 - * FIRE SENSOR # 3-------------.........................
36 - * FIRE SENSOR # 4-------------.........................
49 - * SPECIAL SENSOR # 1----------.........................
50 - * SPECIAL SENSOR # 2----------.........................
65 - * ENTRANCE CONTROL # 1 PANIC--.........................
66 - * ENTRANCE CONTROL # 2 PANIC--.........................
69 - * ENTRANCE CONTROL # 1 TAMPER-.........................
70 - * ENTRANCE CONTROL # 2 TAMPER-.........................
73 - * PROCESSOR OR BELL TAMPER----.........................
74 - * JAMMING DETECTOR FOR EITHER POWER LINE OR MODEM
     (INTERNAL SENSOR ALREADY IN PROCESSOR)
   * NOTE: - FLASHING DIGIT DISPLAY INDICATES AN ALARM
           - STEADY DIGIT DISPLAY INDICATES A NON-REPORTING
             SENSOR OR A SENSOR LEFT IN THE ALARM STATE
------SYSTEM & USER ERRORS-------
80 - CAUTION - FAILURE IN ENTRANCE CONTROL # 1 COMMUNICATION
81 - CAUTION - FAILURE IN ENTRANCE CONTROL # 2 COMMUNICATION
84 - ARMING ABORTED - SYSTEM WILL NOT ARM FROM PROCESSOR
                      (ONLY AT AN ENTRANCE CONTROL) IN
                      LOCAL ALARM, LOCAL/REMOTE, OR REMOTE
                      MODES
85 - CAUTION - SYSTEM ARMED FROM PROCESSOR IN TEST OR
               LOCAL ALERT MODES
86 - CAUTION - POWER LINE OR MODEM RECEIVER PARITY ERROR OR
               SENSORS REPORTING WHICH ARE NOT RECOGNIZED BY
               THE SYSTEM (CODE PLUGS ARE STILL IN PROCESSOR)
87 - CAUTION - POWER HAS BEEN RESTORED
88 - CAUTION - SYSTEM ARMED FROM AN ENTRANCE CONTROL IN
               LOCAL ALERT MODE
89 - ARMING ABORTED - SYSTEM WILL NOT ARM FROM AN ENTRANCE
               CONTROL IN FIRE/PANIC, TEST, OR ACCESS MODES
```

FILE = BASCP

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PAGE = 1        7/ 2/76        15:21:19
 ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

                        ; BAS    4/20/76
                        ;INTEL 8080 PROGRAM FOR CENTRAL PROCESSOR
                        ;TURN OFF ALARMS AND LIGHTS
 0000 3EFD                      MVI   A,0FDH
 0002 D330                      OUT   30H
 0004 32320C                    STA   OUTAL
                        ;SET STACK POINTER
 0007 310E0C                    LXI   SP,SK+14
                        ;INITIALIZE RAM
 000A 210E0C                    LXI   H,KOLD
 000D 11930C                    LXI   D,SENSOR
 0010 0E20                      MVI   C,32
 0012 AF                        XRA   A
 0013 47                        MOV   B,A
 0014 3D                        DCR   A
 0015 70                INT1:   MOV   M,B
 0016 12                        STAX  D
 0017 13                        INX   D
 0018 23                        INX   H
 0019 0D                        DCR   C
 001A C21500                    JNZ   INT1          ;SET TO ZERO AND 0FFH
 001D 0E04                      MVI   C,4
 001F 3C                        INR   A
 0020 3C                        INR   A
 0021 77                INT2:   MOV   M,A
 0022 23                        INX   H
 0023 0D                        DCR   C
 0024 C22100                    JNZ   INT2          ;SET TO 1
 0027 23                        INX   H
 0028 0E09                      MVI   C,9
 002A 3D                        DCR   A
 002B 3D                        DCR   A
 002C 77                INT3:   MOV   M,A
 002D 23                        INX   H
 002E 0D                        DCR   C
 002F C22C00                    JNZ   INT3          ;SET TO FF
 0032 D320                      OUT   20H           ;CLEAR MODE OUTPUT
 0034 CDD60A                    CALL  READCP        ;READ CODE PLUGS
 0037 CD6909                    CALL  IOPR1         ;CLEAR RECEIVER MESSAGE BUFFER
 003A 21CF0C                    LXI   H,TIST
 003D AF                        XRA   A
 003E 77                        MOV   M,A           ;TOP OF TI STACK IS ZERO
 003F 22500C                    SHLD  TISP
 0042 21B400                    LXI   H,180
 0045 22430C                    SHLD  TJAM
 0048 212C01                    LXI   H,300
 004B 22450C                    SHLD  MIN5
 004E 21100E                    LXI   H,3600
 0051 22470C                    SHLD  HOUR
                        ;SET POWER UP  BIT
 0054 3E01                      MVI   A,1
 0056 32520C                    STA   FPOW
                        ;SET TROUBLE BIT
 0059 3E57                      MVI   A,87          ;ERROR CODE FOR LED DISPLAY
 005B CD3A04                    CALL   TIERR        ;STACK CODE AND SET TROUBLE LIGHT
```

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ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

                 ;CHECK FOR RUN SWITCH ON WHEN 1ST POWER UP
005E 21530C              LXI  H,FRUN
0061 3601                MVI  M,1         ;SET RUN-SWITCH-ON FLAG
0063 DB70                IN   70H         ;INPUT RUN SWITCH
0065 E604                ANI  4           ;MASK IN RUN SWITCH
0067 CA1B03              JZ   RUNON       ;IF RUN SWITCH ON, THEN GO TO RUNON
                 ;WAIT FOR RUN SWITCH TO GO ON
006A DB70        WAIT:   IN   70H
006C E604                ANI  4
006E C26A00              JNZ  WAIT        ;IF RUN SWITCH OFF, THEN GO TO WAIT
0071 3600                MVI  M,0         ;RESET RUN SWITCH FLAG
                 ;START ACCESS PERIOD
0073 3E00        SACC:   MVI  A,0         ;DISABLE TAMPER
0075 32150C              STA  FTAMP
0078 2A130C              LHLD TIME        ;START ACCESS TIMER
007B 113C00              LXI  D,60        ;LOAD D,E WITH 60 SEC
007E 19                  DAD  D           ;ADD D,E TO PRESENT TIME
007F 225F0C              SHLD TACC        ;STORE TIME + 60 AT TACC
0082 21280C              LXI  H,FTACC
0085 3601                MVI  M,1         ;SET ACCESS TIMER FLAG ON
0087 AF                  XRA  A
0088 324E0C              STA  X           ;X = 0
008B 32190C              STA  CET         ;RESET TI CODE FOR INTRUSION
008E 11320C              LXI  D,OUTAL
0091 1A                  LDAX D           ;LOAD PRESENT STATE OF ALARMS AND LIGHTS
0092 E6DF                ANI  0DFH        ;TURN ON ACCESS LIGHT
0094 12                  STAX D
0095 D330                OUT  30H
0097 47                  MOV  B,A
0098 3A180C              LDA  FTSW        ;CHECK FOR TAMPER ALARM AT PROCESSOR
009B 4F                  MOV  C,A
009C 3A260C              LDA  ALP         ;IS TAMPER ALARM IN PROGRESS
009F 0F                  RRC
00A0 A1                  ANA  C
00A1 C2C100              JNZ  CKEY        ;IF TAMPER THEN DO NOT TURN OFF TIMER AND ALARMS
00A4 78                  MOV  A,B         ;LOAD PRESENT STATE OF ALARMS
00A5 F6DC                ORI  0DCH        ;TURN ON ACCES LIGHT, OFF ALLARMS
00A7 12                  STAX D           ;STORE NEW STATE OF LIGHTS AND ALARMS
00A8 D330                OUT  30H         ;OUTPUT TO HARDWARE
00AA AF                  XRA  A
00AB 32180C              STA  FTSW        ;RESET TAMPER SWITCH
00AE 32260C              STA  ALP         ;TURN OFF ALARM INPROGRESS AND ALARM FLAGS
00B1 32250C              STA  ALARM
00B4 1605                MVI  D,5         ;TURN OFF ALL TIMERS EXCEPT ACCESS
00B6 23          SACC1:  INX  H
00B7 77                  MOV  M,A
00B8 15                  DCR  D
00B9 C2B600              JNZ  SACC1       ;END LOOP THAT TURNS TIMER FLAGS OFF
00BC 23                  INX  H
00BD 3C                  INR  A
00BE 77                  MOV  M,A         ;RESET SPECIAL ALERT COUNTER TO 1
00BF 23                  INX  H
00C0 77                  MOV  M,A         ;SET ORIGINAL ALERT CNT TO 1
                 ;READ PANEL KEYS
00C1 CDFA08      CKEY:   CALL IOPOLL
```

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ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

00C4 DB20                  IN   20H         ;READ KEYS 0,8,4,2,*,7,4,1
00C6 5F                    MOV  E,A         ;MOVE KEYS TO REG E
00C7 2F                    CMA
00C8 47                    MOV  B,A
00C9 DB30                  IN   30H         ;READ KEYS #,9,6,3
00CB E60F                  ANI  0FH
00CD 57                    MOV  D,A         ;MOVE TO REG D
00CE EE0F                  XRI  0FH
00D0 B0                    ORA  B
00D1 C23707                JNZ  KEY         ;IF A KEY IS DEPRESSED, GO TO CHECK KEY COMB.
00D4 EB                    XCHG
00D5 220E0C                SHLD KOLD        ;ELSE STORE NEW KEY UPDATE
                   ;CHECK FOR PRESENTS OF RECEIVER DATA
00D8 CDFA08        CREC:   CALL IOPOLL
00DB 21230C                LXI  H,FREC      ;IS THERE RECEIVER DATA?
00DE 7E                    MOV  A,M
00DF 3D                    DCR  A
00E0 CAD804                JZ   RECDAT      ;IF THERE IS A MESSAGE, GO TO CHECK TYPE FIELD
                   ;CHECK ARM BUTTON
00E3 CDFA08        CARM:   CALL IOPOLL
00E6 213B0C                LXI  H,ABOLD     ;LOAD OLD ARM BUTTON
00E9 46                    MOV  B,M
00EA DB70                  IN   70H         ;INPUT ARM BUTTON
00EC 77                    MOV  M,A         ;STORE NEW ARM BUTTON
00ED A8                    XRA  B
00EE A0                    ANA  B
00EF 07                    RLC
00F0 DC7404                CC   ARMBUT      ;IF ARM BUTTON PRESSED, GO TO ARMBUT
                   ;CHECK FOR TAMPER
00F3 CDFA08        CTAMP:  CALL IOPOLL
00F6 DB30                  IN   30H         ;INPUT TAMPER SWITCH
00F8 0F                    RRC
00F9 0F                    RRC
00FA 0F                    RRC
00FB 0F                    RRC
00FC E601                  ANI  1
00FE 57                    MOV  D,A
00FF 3A150C                LDA  FTAMP       ;LOAD TAMPER ENABLE FLAG
0102 4F                    MOV  C,A
0103 3A280C                LDA  FTACC       ;LOAD ACCESS TIME FLAG
0106 B2                    ORA  D
0107 B1                    ORA  C
0108 CAAD02                JZ   ENDACC      ;IF ALL FLAGS ARE ZERO, THEN GO TO END ACCESS
010B 21180C                LXI  H,FTSW      ;LOAD TAMPER SWITCH
010E 7A                    MOV  A,D
010F 1E88                  MVI  E,136       ;E = ERROR CODE FOR TAMPER
0111 A1                    ANA  C           ;AND TAMPER SWITCH WITH ENABLE FLAG
0112 CA1B01                JZ   CTIM        ;IF RESULT IS 1, THEN ALARM
0115 35                    DCR  M
0116 3601                  MVI  M,1
0118 C20F06                JNZ  GART        ;GO TO TAMPER ALARM
                   ;CHECK TIMERS
011B 79            CTIM:   MOV  A,C         ;CHECK TAMPER ENABLE
011C 0F                    RRC              ;IF DISABLED THEN OUTPUT MODE LEDS
011D DA2601                JC   CTIM1
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ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

0120 CD990B                 CALL READM      ;READ MODE SWITCH
0123 2F                     CMA
0124 D320                   OUT  20H        ;OUTPUT TO LEDS
0126 01270C       CTIM1:    LXI  B,FTACC-1  ;H,L = ADDR OF TIMER FLAGS
0129 2A5F0C                 LHLD TACC       ;IS TIME EXPIRED ON 60 SEC ACCESS TIMER?
012C CDD302                 CALL CKTIM
012F D23301                 JNC   CT1       ;IF NOT THEN NEXT TIMER
0132 02                     STAX B          ;TURN OFF TIMER
0133 3A170C       CT1:      LDA  ARMS       ;IS SYSTEM ARMED?
0136 0F                     RRC
0137 3F                     CMC
0138 1F                     RAR
0139 0F                     RRC
013A 57                     MOV  D,A        ;OUTPUT ARM STATUS TO LED
013B 21320C                 LXI  H,OUTAL    ;TURN ON ARMLIGHT IF ARMED
013E 7E                     MOV  A,M
013F E6BF                   ANI  0BFH
0141 B2                     ORA  D
0142 77                     MOV  M,A
0143 D330                   OUT  30H
0145 2A610C       CT2:      LHLD TCODE      ;CHECK 2 SEC CODE TIMER
0148 CDD302                 CALL CKTIM
014B D25201                 JNC   CT3
014E 02                     STAX B
014F C3D703                 JMP  ERREC      ;IF TIME EXPIRED, THEN GO TO ERREC(EC ERROR)
0152 03           CT3:      INX  B          ;CHECK DISPLAY TIMER
0153 0A                     LDAX B
0154 A7                     ANA  A
0155 CA8401                 JZ   CT4
0158 3A5A0C                 LDA  TISO       ;CHECK TO SEE IF PANEL SHOULD BLINK
015B A7                     ANA  A
015C FA7501                 JM   CT3B
015F CA7501                 JZ   CT3B
0162 E67F                   ANI  7FH
0164 CDC304                 CALL BCD
0167 57                     MOV  D,A
0168 3A120C                 LDA  TCNT       ;IF SO, THEN BLINK EVERY HALF SEC
016B E610                   ANI  10H
016D 7A                     MOV  A,D
016E CA7301                 JZ   CT3A       ;EVERY HALF SEC., COMPLIMENT MODE SWITCH LEDS
0171 3EFF                   MVI  A,0FFH
0173 D340         CT3A:     OUT  40H
0175 2A630C       CT3B:     LHLD TDISP
0178 CDDE02                 CALL CTIME
017B C28401                 JNZ  CT4
017E 02                     STAX B
017F 3D                     DCR  A
0180 D320                   OUT  20H        ;TURN OFF MODE LEDS
0182 D340                   OUT  40H        ;BLANK OUT TI LEDS
0184 03           CT4:      INX  B          ;CHECK FIRE ALARM TIMER
0185 0A                     LDAX B
0186 A7                     ANA  A
0187 CABB01                 JZ   CT5
018A 21490C                 LXI  H,FIRBEL   ;LOAD FIRE BELL ALARM FLAG
018D 5E                     MOV  E,M
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ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

018E 21320C       221          LXI  H,OUTAL     ;TURN ON AND OFF BELL EVERY SEC
0191 7E           222          MOV  A,M
0192 E6E3         223          ANI  0E3H
0194 57           224          MOV  D,A
0195 3A120C       225          LDA  TCNT
0198 0F           226          RRC
0199 0F           227          RRC
019A 0F           228          RRC
019B 0F           229          RRC
019C E604         230          ANI  4
019E B3           231          ORA  E
019F B2           232          ORA  D
01A0 77           233          MOV  M,A
01A1 D330         234          OUT  30H
01A3 2A650C       235          LHLD TFIRE
01A6 CDDE02       236          CALL CTIME
01A9 C2BB01       237          JNZ  CT5
01AC 02           238          STAX B
01AD 21320C       239          LXI  H,OUTAL
01B0 7E           240          MOV  A,M
01B1 F61C         241          ORI  1CH         ;IF TIMER EXPIRED, THEN TURN OFF ALARMS
01B3 77           242          MOV  M,A
01B4 D330         243          OUT  30H
01B6 3E0F         244          MVI  A,0FH
01B8 CD1303       245          CALL RSTAP       ;RESET FIRE ALARM IN PROGESS
01BB 2A5B0C       246 CT5:     LHLD TBEL        ;CHECK BELL TIMER
01BE CDD302       247          CALL CKTIM
01C1 D2D101       248          JNC  CT6
01C4 02           249          STAX B
01C5 21320C       250          LXI  H,OUTAL
01C8 7E           251          MOV  A,M
01C9 F604         252          ORI  4
01CB 77           253          MOV  M,A
01CC D330         254          OUT  30H         ;IF TIMER EXPIRED, THEN TURN OFF BELL
01CE CD1103       255          CALL RSTAL       ;RESET ALARM(PANIC,INTRD,TAMPER)
01D1 2A5D0C       256 CT6:     LHLD TALT        ;CHECK LOCAL ALERT TIMERS
01D4 CDD302       257          CALL CKTIM
01D7 D21102       258          JNC  CT9
01DA 212E0C       259          LXI  H,SALCNT
01DD 7E           260          MOV  A,M         ;IF EXPIRED, THEN DECREMENT SPECIAL CNT
01DE 3D           261          DCR  A
01DF CAE301       262          JZ   CT7         ;IF RESULT IS NOT 0, START ANOTHER 5 SEC ALERT
01E2 77           263          MOV  M,A
01E3 57           264 CT7:     MOV  D,A
01E4 3A300C       265          LDA  ALCNT       ;DECREMENT COUNT
01E7 3D           266          DCR  A
01E8 C2AD06       267          JNZ  MSGB1
01EB B2           268          ORA  D
01EC C2F901       269          JNZ  CT8         ;IF BOTH COUNTERS(ALCNT & SALCNT) = 0, THEN
01EF 02           270          STAX B
01F0 01320C       271          LXI  B,OUTAL     ;TURN OFF ALERT
01F3 0A           272          LDAX B
01F4 F618         273          ORI  18H
01F6 02           274          STAX B
01F7 D330         275          OUT  30H
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ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

01F9 23         276 CT8:    INX  H
01FA 7E         277         MOV  A,M       ;LOAD AND RESET ORIGINAL COUNT
01FB 3600       278         MVI  M,0
01FD FE0F       279         CPI  15        ;IF 1.25 WARNING, THEN ARM
01FF CAC203     280         JZ   SARN      ;GO TO ARM SENSORS
0202 FE05       281         CPI  5
0204 CAF805     282         JZ   GARI      ;IF 20 SEC WARNING, GO TO INTRUSION ALARM
0207 7A         283         MOV  A,D
0208 A7         284         ANA  A
0209 C2B006     285         JNZ  MSGB2     ;IF COUNT = 0 AND SPEC CNT NOT 0, GO TO MSGB
020C 3E1E       286         MVI  A,1EH
020E CD1303     287         CALL RSTAP     ;RESET SPECIAL ALARM IN PROGRESS
0211 CDFA08     288 CT9:    CALL IOPOLL
0214 2A450C     289         LHLD MINS
0217 CDDE02     290         CALL CTIME
021A C24202     291         JNZ  CT10      ;IF 5 MIN. CLOCK EXPIRED, THEN UPDATE STATUS
021D 112C01     292         LXI  D,300
0220 19         293         DAD  D
0221 22450C     294         SHLD MINS
                295 ;ROUTINE THAT UPDATES STATUS BYTES EVERY 5 MIN.
0224 111E00     296         LXI  D,30
0227 2A560C     297         LHLD STSEN     ;H,L = TOP OF STATUS BYTE STACK
022A 3A580C     298         LDA  SENBOT    ;LOAD ACC WITH BOTTOM OF STACK
022D 95         299         SUB  L
022E 3C         300         INR  A         ;ACC = NO. OF BYTES IN STACK
022F 19         301         DAD  D
0230 57         302         MOV  D,A
0231 0607       303         MVI  B,7
0233 0EF7       304         MVI  C,0F7H
0235 7E         305 STM1:   MOV  A,M       ;LOAD STATUS BYTE
0236 5F         306         MOV  E,A
0237 A0         307         ANA  B         ;SHIFT BITS 1,2 LEFT 1 BIT
0238 0F         308         RRC
0239 17         309         RAL            ;MOVE BIT 0 TO BIT 1
023A 8B         310         ADC  E
023B A1         311         ANA  C         ;CLEAR BIT 3
023C 77         312         MOV  M,A       ;RESTORE UPDATED STATUS BYTE
023D 23         313         INX  H
023E 15         314         DCR  D
023F C23502     315         JNZ  STM1      ;IF END OF STACK, THEN END OF LOOP
0242 CDFA08     316 CT10:   CALL IOPOLL
0245 2A470C     317         LHLD HOUR
0248 CDDE02     318         CALL CTIME
024B C29302     319         JNZ  CT11
024E 321B0C     320         STA  ERRCNT    ;RESET RECEIVER ERROR COUNT
0251 11100E     321         LXI  D,3600
0254 19         322         DAD  D
0255 22470C     323         SHLD HOUR
                324 ;STATUS HOURLY UPDATE
                325 ;BIT 7 = STATUS ERROR
                326 ;BIT 6 = PREVIOUS HOUR STATUS
                327 ;BIT 5 = PRESENT HOUR STATUS
                328 ;1ST RESET STATUS TROUBLE
0258 2A540C     329         LHLD HRSEN     ;B,C = SENSOR ARRAY
025B 44         330         MOV  B,H
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ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

025C 4D                  MOV   C,L
025D 211E00              LXI   H,30
0260 3A580C              LDA   SENBOT
0263 91                  SUB   C
0264 3C                  INR   A          ;ARRAY COUNT
0265 09                  DAD   B
0266 EB                  XCHG
0267 323C0C     STU1:    STA   COUNT
026A 0A                  LDAX  B          ;LOAD SENSOR BYTE
026B 3C                  INR   A
026C CA8A02              JZ    STU3       ;IF SENSOR SEPERATOR THEN GO TO NEXT SENSOR
026F 1A                  LDAX  D          ;LOAD STATUS BYTE
0270 67                  MOV   H,A        ;IF BITS 1 OR 2 ARE 0,
0271 E6E0                ANI   0E0H
0273 84                  ADD   H          ;SHIFT BITS 5-7 LEFT
0274 F620                ORI   20H        ;BIT 5 = 1
0276 12                  STAX  D
0277 0A                  LDAX  B
0278 C680                ADI   128        ;GENERATE STATUS ERROR CODE
027A CD3A04              CALL  TIERR      ;STACK ERROR CODE ON TI STACK
027D 42                  MOV   B,D
027E 1A                  LDAX  D
027F C5                  PUSH  B
0280 D5                  PUSH  D
0281 A7                  ANA   A          ;IF STATUS ERROR THEN GO TO NEXT BYTE
0282 F40903              CP    RSTB       ;NO STATUS TROUBLE AND ERASE CODE FROM STACK
0285 CDFA08              CALL  IOPOLL
0288 D1                  POP   D
0289 C1                  POP   B
028A 13         STU3:    INX   D          ;GO TO NEXT STATUS BYTE
028B 03                  INX   B
028C 3A3C0C              LDA   COUNT
028F 3D                  DCR   A
0290 C26702              JNZ   STU1       ;END OF STATUS UPDATE LOOP
0293 2A430C     CT11:    LHLD  TJAM
0296 CDDE02              CALL  CTIME
0299 C2C100              JNZ   CKEY       ;IF NO JAMMING GO TO CHECK KEY INPUT
029C 018900              LXI   B,137
029F 09                  DAD   B
02A0 22430C              SHLD  TJAM
02A3 51                  MOV   D,C        ;SET ALARM BITS AND ERROR CODE FOR JAMMING
02A4 21110C              LXI   H,FJAM
02A7 96                  SUB   M
02A8 3F                  CMC
02A9 72                  MOV   M,D
02AA C34605              JMP   RDJAM      ;JAMMING IS AN ITRUSION (INTERIOR) ALARM
                ;END OF ACCESS PERIOD ROUTINE
02AD CDD60A     ENDACC:  CALL  READCP     ;READ CODEPLUGS
02B0 21320C              LXI   H,OUTAL    ;TURN OFF ACCESS LIGHT
02B3 7E                  MOV   A,M
02B4 F620                ORI   20H
02B6 77                  MOV   M,A
02B7 D330                OUT   30H
02B9 3E01                MVI   A,1
02BB 32150C              STA   FTAMP      ;ENABLE TAMPER
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ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

02BE 3D          386          DCR   A
02BF 3D          387          DCR   A
02C0 D320        388          OUT   20H          ;CLEAR MODE OUTPUT
02C2 3A520C      389          LDA   FPOW         ;CHECK POWER UP BIT
02C5 A7          390          ANA   A
02C6 C22303      391          JNZ   SARK         ;START EC HANDSHAKE
02C9 3A4E0C      392          LDA   X
02CC A7          393          ANA   A
02CD C28003      394          JNZ   SARL         ;IF X = 1, GO TO SENSOR ARMING
02D0 C3D800      395          JMP   CREC         ;ELSE GO TO MAIN LOOP
                 396 ;CHECK TO SEE IF TIMER IS ON
02D3 C5          397 CKTIM:   PUSH B
02D4 E5          398          PUSH H
02D5 CDFA08      399          CALL  IOPOLL
02D8 E1          400          POP   H
02D9 C1          401          POP   B
02DA 03          402          INX   B
02DB 0A          403          LDAX  B
02DC A7          404          ANA   A
02DD C8          405          RZ                 ;RETURN IF TIMER IS OFF
                 406 ;ROUTINE THAT CHECKS TO SEE IF H,L = TIME
                 407 ;ZERO FLAG SET ON RETURN IF H,L = TIME
02DE EB          408 CTIME:   XCHG
02DF 2A130C      409          LHLD  TIME
02E2 7B          410          MOV   A,E
02E3 95          411          SUB   L
02E4 A7          412          ANA   A            ;CLEAR CARRY
02E5 C0          413          RNZ
02E6 7A          414          MOV   A,D
02E7 94          415          SUB   H
02E8 A7          416          ANA   A            ;RESET CARRY
02E9 C0          417          RNZ
02EA 37          418          STC
02EB C9          419          RET
                 420 ;ROUTINE THAT TAKES THE NO. IN B,0 AND DELETES
                 421 ;ALL TI ERROR CODES BETWEEN B AND 0 (DELETE Y, IF B > Y > 0)
02EC 21CF0C      422 RTI:     LXI   H,TIST       ;LOAD TOP OF TI STACK
02EF 4D          423          MOV   C,L
02F0 54          424          MOV   D,H
02F1 5D          425          MOV   E,L          ;D,E = H,L
02F2 7E          426 RTI1:    MOV   A,M          ;LOAD ERROR CODE
02F3 23          427          INX   H
02F4 B8          428          CMP   B
02F5 DAFA02      429          JC    RT2          ;IF CODE < B, DO NOT RESTORE
02F8 12          430          STAX  D            ;ELSE CODE >= B
02F9 13          431          INX   D
02FA A7          432 RT2;     ANA   A
02FB C2F202      433          JNZ   RTI1         ;IS END OF STACK, THEN END TI RESET
02FE 12          434          STAX  D            ;STORE END OF STACK
02FF 79          435 RSTIB:   MOV   A,C          ;CHECK IF THERE ARE NO ERROR CODES
0300 32500C      436          STA   TISP         ;SET TI STACK POINTER AT TOP
0303 95          437          SUB   L
0304 C0          438          RNZ                ;IF NO ERROR CODES THEN RESET TI BIT
0305 321A0C      439          STA   TIBIT
0308 C9          440          RET
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ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

                441 ;RESET TI BIT IF NO ERROR CODES
0309 3600       442 RSTB:    MVI  M,0          ;RESET ERROR CODE
030B 01CF0C     443          LXI  B,TIST
030E C3FF02     444          JMP  RSTIB
                445 ;RESET ALARM IN PROGRESS
0311 3E11       446 RSTAL:   MVI  A,11H
0313 EB         447 RSTAP:   XCHG
0314 21260C     448          LXI  H,ALP
0317 A6         449          ANA  M
0318 77         450          MOV  M,A
0319 EB         451          XCHG
031A C9         452          RET
                453 ;IF POWER SWITCH IS ON WHEN FIRST COMING UP THEN THIS ROUTINE IS EXECUTED
031B 3E01       454 RUNON:   MVI  A,1          ;ACC = 1
031D 324E0C     455          STA  X            ;X = 1
0320 32150C     456          STA  FTAMP        ;ENABLE TAMPER
0323 21930C     457 SARK:    LXI H,SENSOR      ;LOAD EC STACK POINTER
0326 224A0C     458          SHLD ECSS         ;STORE AS THE START OF STACK
0329 C33B03     459          JMP  SAR1
032C 2A4A0C     460 SARM:    LHLD ECSS         ;LOAD EC STACK START
032F EB         461          XCHG
0330 2A4C0C     462          LHLD ECSP         ;LOAD STACK PTR AND COMPARE TO SEE IF END OF STACK
0333 CDCA03     463          CALL ECSU         ;UPDATE STACK POINTER
0336 7B         464          MOV  A,E
0337 BD         465          CMP  L            ;IF ECSP = ECSS, THEN END OF STACK
0338 CA6E03     466          JZ   SAR3         ;IF STACK EMPTY THEN GO TO SAR3
033B 7E         467 SAR1:    MOV  A,M          ;LOAD EC NO.
033C 3C         468          INR  A            ;CHECK TO SEE IF NO. OF EC = 0
033D CA6E03     469          JZ   SAR3         ;IF YES THEN STACK EMPTY, GO TO SAR3
0340 3D         470          DCR  A
0341 E607       471 SAR2:    ANI  7
0343 F608       472          ORI  8
0345 57         473          MOV  D,A          ;TRANSMIT 1ST HALF CODE WORD
0346 3A120C     474          LDA  TCNT         ;GENERATE RANDOM NO. FROM TIME COUNT
0349 32420C     475          STA  CODE
034C E60F       476          ANI  0FH
034E 5F         477          MOV  E,A
034F 7A         478          MOV  A,D
0350 1601       479          MVI  D,1
0352 CD710A     480          CALL TRANS
0355 23         481          INX  H            ;START 2 SEC CODE TIMER
0356 2A130C     482          LHLD TIME
0359 23         483          INX  H
035A 23         484          INX  H
035B 22610C     485          SHLD TCODE
035E 3E01       486          MVI  A,1
0360 32290C     487          STA  FTCODE
0363 32160C     488          STA  VARM         ;VARM = 1 , REP = 4
0366 3E04       489          MVI  A,4
0368 32310C     490          STA  REP
036B C3C100     491          JMP  CKEY
                492 ;END OF EC STACK, CHECK FOR POWER BIT(IS THIS THE 1ST TIME)
036E 21520C     493 SAR3:    LXI  H,FPOW       ;ACC = POWER BIT
0371 7E         494          MOV  A,M
0372 A7         495          ANA  A
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ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

0373 CAAE03        496          JZ   SAR6        ;IF POWER BIT NOT ON THEN GO TO SAR6
0376 AF            497          XRA  A
0377 77            498          MOV  M,A         ;RESET POWER BIT
0378 21530C        499          LXI  H,FRUN      ;IF RUN BIT ON THEN GO TO SAR5
037B 35            500          DCR  M
037C CAA403        501          JZ   SAR5
037F 34            502          INR  M
                   503 ;CHECK FOR USER ERROR
0380 3A4F0C        504 SARL:    LDA  MODE        ;LOAD ALARM MODE
0383 E6C0          505          ANI  0C0H        ;IF MODE 1 OR 2
0385 C29903        506          JNZ  SAR4        ;IF MODE = 1 OR 2, THEN SET TIBIT
0388 3A930C        507          LDA  SENSOR      ;LOAD TOP OF EC STACK
038B 3C            508          INR  A           ;IF ACC = FF THEN NO. OF EC = 0
038C 0664          509          MVI  B,100
038E CAA103        510          JZ   SAR5A       ;IF TOP IS AN END OF EC FLAG, SKIP ERROR OUTPUT
0391 3E54          511          MVI  A,84        ;ERROR CODE FOR TI
0393 CD3A04        512          CALL TIERR
0396 C3D800        513          JMP  CREC        ;RETURN TO MAIN LOOP
0399 3E55          514 SAR4:    MVI  A,85        ;OUTPUT ERROR CODE
039B CD3A04        515          CALL TIERR
039E C3A403        516          JMP  SAR5
03A1 CDEC02        517 SAR5A:   CALL RTI         ;RESET TI CODES
03A4 CDFA08        518 SAR5:    CALL IOPOLL
03A7 CDF306        519          CALL MASK        ;MASK OUT ALL BAD SENSORS
03AA A7            520          ANA  A
03AB CAD800        521          JZ   CREC        ;IF NO. OF SENSORS IN SYSTEM = 0, DO NOT ARM
03AE CDFA08        522 SAR6:    CALL IOPOLL
03B1 3A4E0C        523          LDA  X           ;ACC = X
03B4 A7            524          ANA  A
03B5 CAD800        525          JZ   CREC        ;IF X = 0, DO NOT ARM
03B8 3A4F0C        526          LDA  MODE
03BB E6C0          527          ANI  0C0H        ;CHECK FOR ALARM MODE
                   528                           ;ALARM MODE 1 OR 2, ARM IMMEDIATLY
03BD 3E0F          529          MVI  A,15        ;ELSE GIVE A 1.25 MIN. WARNING
03BF CAAA06        530          JZ   MSGB        ;ON LOCAL ALERT, BEFORE ARMING
                   531 ;ARM IMMEDIATELY
03C2 3E01          532 SARN:    MVI  A,1
03C4 32170C        533          STA  ARMS        ;ARM SENSOR
03C7 C3D800        534          JMP  CREC
                   535 ;UPDATE EC STACK(INCREMENT STACK)
03CA 23            536 ECSU:    INX  H
03CB 7E            537          MOV  A,M
03CC 3C            538          INR  A
03CD C2D303        539          JNZ  ECSU1       ;IF H,L + 1 IS BELOW LIMIT
03D0 21930C        540          LXI  H,SENSOR    ;NEW POINTER = TOP OF STACK
03D3 224C0C        541 ECSU1:   SHLD ECSP        ;STORE NEW STACK POINTER
03D6 C9            542          RET
                   543 ;EC ERROR IF CODE TIMER ELAPSES
03D7 3A160C        544 ERREC:   LDA  VARM        ;LOAD VARM
03DA 7A            545          MOV  A,D
03DB 3A420C        546          LDA  CODE
03DE 15            547          DCR  D
03DF CAE603        548          JZ   ERREC1      ;LOAD 1ST OR 2ND HALF CODE WORD
03E2 07            549          RLC
03E3 07            550          RLC
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ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

03E4 07             551            RLC
03E5 07             552            RLC
03E6 E60F           553 ERREC1: ANI   0FH
                    554 ;ERROR IN EC HANDSHAKE
03E8 5F             555 ECERR:  MOV   E,A
03E9 3A310C         556         LDA   REP          ;IS REP = 0
03EC 3D             557         DCR   A
03ED C20204         558         JNZ   ECERR1       ;IF 0, GO TO NEXT EC
03F0 2A4C0C         559         LHLD  ECSP         ;GENERATE ERROR CODE
03F3 7E             560         MOV   A,M
03F4 C650           561         ADI   80
03F6 EB             562         XCHG
03F7 CD3A04         563         CALL  TIERR
03FA EB             564         XCHG
03FB AF             565         XRA   A
03FC 32160C         566         STA   VARM         ;RESET VARM
03FF C32C03         567         JMP   SARM
0402 32310C         568 ECERR1: STA   REP          ;STORE REP - 1
0405 2A610C         569         LHLD  TCODE        ;START CODE TIMER
0408 7B             570         MOV   A,E
0409 23             571         INX   H
040A 23             572         INX   H
040B 22610C         573         SHLD  TCODE
040E 5F             574         MOV   E,A
040F 3E01           575         MVI   A,1
0411 32290C         576         STA   FTCODE
0414 3A160C         577         LDA   VARM
0417 57             578         MOV   D,A
0418 2A4C0C         579         LHLD  ECSP
041B 7E             580         MOV   A,M
041C E60F           581         ANI   0FH
041E F608           582         ORI   8
0420 CD710A         583         CALL  TRANS        ;RETRANSMIT MESSAGE
0423 C3E300         584         JMP   CARM
                    585 ;UPDATE TI STACK POINTER
0426 7E             586 TISU:   MOV   A,M          ;GO TO TOP IF PRESENT OR NEXT CODE IS ZERO
0427 A7             587         ANA   A
0428 CA3104         588         JZ    TISU0
042B 23             589         INX   H
042C 7E             590         MOV   A,M
042D A7             591         ANA   A
042E C23404         592         JNZ   TISU1
0431 21CF0C         593 TISU0:  LXI   H,TIST
0434 22500C         594 TISU1:  SHLD  TISP
0437 C9             595         RET
                    596 ;TIERR: ROUTINE THAT STACKS THE ERROR CODE IN ACC
                    597 ;     . ONTO THE TROUBLE INDICATOR LED OUTPUT STACK
                    598 ;TIERR WILL ALSO SET TROUBLE BIT
0438 D63F           599 TIERRA: SUI   63           ;ADJUST SENSOR NO. TO ERROR CODE
043A 47             600 TIERR:  MOV   B,A
043B 3E0F           601         MVI   A,0FH
043D 321A0C         602         STA   TIBIT        ;SET TROUBLE BIT
0440 21CE0C         603         LXI   H,TISTM      ;H,L = TOP OF TI(TROUBLE INDICATOR STACK)
0443 23             604 TIERR1: INX   H            ;LOOP THAT CHECKS TO SEE IF ERROR IS
0444 7E             605         MOV   A,M          ;NOT ALREADY IN TI STACK
```

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ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

0445 A7                    ANA  A          ;IF END OF STACK CHECK FOR END OF RAM
0446 CA5704                JZ   TIERR3     ;GO TO TIERR3 ON END OF STACK
0449 B8                    CMP  B
044A C24304                JNZ  TIERR1     ;IF CODES NOT = THEN GO TO NEXT TI CODE
044D 23           TIERR2:  INX  H          ;ELSE DELETE CODE FROM STACK
044E 7E                    MOV  A,M
044F 2B                    DCX  H
0450 77                    MOV  M,A        ;MOVE ALL SUCCEDING CODES UP 1
0451 23                    INX  H
0452 A7                    ANA  A
0453 C24D04                JNZ  TIERR2     ;IF NO END OF STACK MOVE NEXT CODE UP
0456 2B                    DCX  H
0457 7D           TIERR3:  MOV  A,L        ;CHECK FOR END OF RAM
0458 3C                    INR  A
0459 C26E04                JNZ  TIERR5     ;IF NOT END OF RAM THEN STACK ERROR CODE AT BOTTOM
045C 78                    MOV  A,B        ;IF ERROR CODE IS NOT ALARM, THEN RETURN
045D FE64                  CPI  100
045F D0                    RNC
0460 21CE0C                LXI  H,TISTM    ;IF END OF TI STACK THEN STACK ONLY ALARMS
0463 23           TIERR4:  INX  H
0464 7E                    MOV  A,M                  ;CHECK FOR A NON ALARM CODE
0465 FE64                  CPI  100
0467 C26304                JNZ  TIERR4     ;IF NOT AN ALARM CODE THEN CHECK NEXT CODE
046A 70                    MOV  M,B        ;REPLACE ERROR CODE WITH NEW
046B 2EFF                  MVI  L,0FFH     ;PUT TI ADDR AT BOTTOM OF RAM
046D C9                    RET
046E 70           TIERR5:  MOV  M,B        ;WRITE ERROR CODE AT BOTTOM OF STACK
046F 23                    INX  H
0470 3600                  MVI  M,0        ;SET NEW END OF STACK
0472 2B                    DCX  H
0473 C9                    RET
                  ;ARMBUT: OUTPUT TROUBLE TO LED AND ENDS ACCESS PERIOD
0474 3A150C       ARMBUT:  LDA  FTAMP      ;LOAD TAMPER EN/DIS
0477 A7                    ANA  A
0478 C28304                JNZ  AB1        ;IF TAMPER DISALBED, THEN ENABLE END ACCESS
047B AF                    XRA  A
047C 32280C                STA  FTACC      ;END ACCESS TIMER
047F 3C                    INR  A
0480 324E0C                STA  X          ;X = 1
0483 2A500C       AB1:     LHLD TISP       ;LOAD H,L WITH PRESENT TI STACK PTER.
0486 7E                    MOV  A,M
0487 4F                    MOV  C,A
0488 1664                  MVI  D,100
048A BA                    CMP  D
048B DA9604                JC   AB3        ;IF ERROR CODE > 100, THEN SUBTRACT 100
048E 1EBF                  MVI  E,191
0490 BB                    CMP  E
0491 DA9504                JC   AB2        ;IF NOT STATUS ERROR CODE, THEN DO NOT SUBTR
0494 53                    MOV  D,E
0495 92           AB2:     SUB  D
0496 47           AB3:     MOV  B,A
0497 79                    MOV  A,C
0498 FE4B                  CPI  75
049A 78                    MOV  A,B
049B DAA004                JC   AB4        ;IF ALARM ERROR CODE, THEN BLINK TI LED
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 ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

 049E F680         661          ORI  80H
 04A0 325A0C       662 AB4:     STA  TISO        ;STORE NEW ERROR CODE
 04A3 E67F         663          ANI  7FH
 04A5 CDC304       664          CALL BCD
 04A8 D340         665          OUT  40H
 04AA CD2604       666          CALL TISU        ;UPDATE STACK(INCR STACK POINTER)
 04AD 3A4F0C       667          LDA  MODE
 04B0 2F           668          CMA
 04B1 D320         669          OUT  20H         ;LIGHT MODE LEDS
 04B3 2A130C       670          LHLD TIME        ;START ARM LIGHT 20 SEC TIMER
 04B6 111400       671          LXI  D,20
 04B9 19           672          DAD  D
 04BA 22630C       673          SHLD TDISP
 04BD 3E01         674          MVI  A,1
 04BF 322A0C       675          STA  FTDISP
 04C2 C9           676          RET
                   677 ;BCD: CONVERTS ACC FROM BINARY TO BCD
 04C3 57           678 BCD:     MOV  D,A
 04C4 E6F0         679          ANI  0F0H
 04C6 07           680          RLC
 04C7 07           681          RLC
 04C8 07           682          RLC
 04C9 07           683          RLC
 04CA 5F           684          MOV  E,A         ;E = NO. OF 16'S
 04CB 7A           685          MOV  A,D
 04CC 1606         686          MVI  D,6
 04CE 92           687          SUB  D
 04CF 82           688 BCD1:    ADD  D           ;LOOP THAT ADDS 6 FOR E TIMES
 04D0 B7           689          ORA  A           ;CLEAR AUX. CARRY
 04D1 27           690          DAA              ;DECICMAL ADJUST
 04D2 1D           691          DCR  E
 04D3 F2CF04       692          JP   BCD1        ;END LOOP
 04D6 27           693          DAA
 04D7 C9           694          RET
                   695 ;MESSAGE DECODING ROUTINE
                   696 ;COMPARES RECEIVER DATA WITH LIST OF SENSORS
 04D8 77           697 RECDAT:  MOV  M,A         ;RESET RECEIVER FLAG
 04D9 21930C       698          LXI  H,SENSOR    ;LOAD TOP OF SENSOR LIST
 04DC 3A370C       699          LDA  TYPE        ;LOAD TYPE FIELD OF RECEIVER DMESSAGE
 04DF E60F         700          ANI  0FH         ;CHECK IF MESSAGE IS FROM AN EC
 04E1 57           701          MOV  D,A
 04E2 7E           702 RD0:     MOV  A,M
 04E3 BA           703          CMP  D
 04E4 CA8A07       704          JZ   INEC        ;IF A MATCH OCCURS THEN JUMP TO CHECK SUB TYPE
 04E7 23           705          INX  H
 04E8 3C           706          INR  A
 04E9 C2E204       707          JNZ  RD0         ;CHECK NEXT SENSOR TIL END OF EC FLAG
 04EC 7A           708          MOV  A,D         ;ROTATE IN ID DATA(BITS 0-3 = ID DATA,
                                                           ;BITS E-7 = TYPE)
 04ED 07           709          RLC
 04EE 07           710          RLC
 04EF 07           711          RLC
 04F0 07           712          RLC
 04F1 57           713          MOV  D,A
 04F2 3A390C       714          LDA  IDDATA
 04F5 E60F         715          ANI  0FH
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 ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

 04F7 B2            716          ORA  D
 04F8 57            717          MOV  D,A
 04F9 3C            718          INR  A
 04FA CA6805        719          JZ   RD3      ;IF SENSOR = FF, THEN GO TO ECERR
 04FD 3D            720          DCR  A
 04FE D640          721          SUI  40H      ;GENERATE ERROR CODE FOR PANIC
 0500 5F            722          MOV  E,A
 0501 CD8B05        723          CALL CSEN     ;CHECK FOR PANIC MESSAGE
 0504 DA1806        724          JC   GARP     ;IF PANIC, GO TO GENERAL ALARM ROUTINE
 0507 7B            725          MOV  A,E
 0508 C27A05        726          JNZ  CARMEE   ;RETURN, NON ALARM MESSAGE
 050B D60C          727          SUI  0CH      ;GENERATE ERROR CODE FOR TAMPER
 050D 5F            728          MOV  E,A
 050E CD8B05        729          CALL CSEN     ;CHECK FOR EC TAMPER MESSAGE
 0511 DA0F06        730          JC   GART     ;IF TAMPER, GO TO TAMPER ALARM
 0514 7B            731          MOV  A,E
 0515 C27A05        732          JNZ  CARMEE   ;RETURN, NON ALARM MESSAGE
 0518 CD8B05        733          CALL CSEN     ;CHECK FOR SPECIAL ALARM MESSAGE
 051B DA0606        734          JC   GARS     ;IF SPECIAL, GO TO SPECIAL ALARM ROUTINE
 051E C26E05        735          JNZ  CARME    ;RETURN, NON ALARM MESSAGE
 0521 D5            736          PUSH D
 0522 E5            737          PUSH H
 0523 CDFA08        738          CALL IOPOLL
 0526 E1            739          POP  H
 0527 D1            740          POP  D
 0528 CD8B05        741          CALL CSEN     ;CHECK FOR PERIMETER ALARM MESSAGE
 052B D24005        742          JNC  RD1      ;IF NO PERIMETER ALARM, GO CHECK OTHER SENSORS
 052E 3A4F0C        743          LDA  MODE     ;ELSE CHECK MODE
 0531 E604          744          ANI  4
 0533 C26E05        745          JNZ  CARME    ;IF FIRE/PANIC MODE, IGNOR MESSAGE AND RETURN
 0536 3A170C        746          LDA  ARMS     ;LOAD SENSORS ARMED FLAG
 0539 A7            747          ANA  A
 053A CA6E05        748          JZ   CARME    ;IF SENSORS NOT ARMED, THEN IGNOR MESSAGE AND RETURN
 053D C36806        749          JMP  INTRD    ;ELSE GO TO INTRUSION ALARM
 0540 C26E05        750 RD1:     JNZ  CARME    ;RETURN, NO ALARM MESSAGE FROM SENSOR
 0543 CD8B05        751          CALL CSEN     ;CHECK FOR INTERNAL ALARM MESSAGE
 0546 D25B05        752 RDJAM:   JNC  RD2      ;IF NO INTERNAL ALARM, CHECK FOR FIRE ALARM
 0549 3A4F0C        753          LDA  MODE     ;CHECK MODE
 054C E601          754          ANI  1
 054E CA6E05        755          JZ   CARME    ;IF NOT SENSOR MODE 3 (ALL), THEN RETURN
 0551 3A170C        756          LDA  ARMS     ;LOAD SENSOR ARMED FLAG
 0554 A7            757          ANA  A
 0555 CA6E05        758          JZ   CARME    ;IF SENSORS NOT ARMED, THE RETURN
 0558 C36806        759          JMP  INTRD    ;GO TO INTRUSION ALARM ROUTINE
 055B C26E05        760 RD2:     JNZ  CARME    ;RETURN, NON ALARM MESSAGE
 055E CD8B05        761          CALL CSEN     ;CHECK FOR FIRE ALARM MESSAGE
 0561 7A            762          MOV  A,D      ;ACC = ERROR CODE
 0562 DAC905        763          JC   FIRE     ;IF FIRE, THEN GO TO FIRE ALARM ROUTINE
 0565 C26E05        764          JNZ  CARME    ;RETURN, NONE ALARM MESSAGE
 0568 CD0B0A        765 RD3:     CALL RECERR   ;IF NO SENSORS MATCH, THEN RECEIVER ERROR
 056B C3E300        766          JMP  CARM     ;RETURN TO MAIN POLLING LOOP
 056E 7A            767 CARME:   MOV  A,D      ;UPDATE STATUS ERROR
 056F C680          768          ADI  128
 0571 CD3A04        769          CALL TIERR    ;STACK ERROR CODE
 0574 59            770          MOV  E,C
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ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

0575 CD0903                CALL RSTB       ;DELETE STATUS ERROR CODE FROM TI STACK
0578 4B                    MOV  C,E
0579 7A                    MOV  A,D        ;CHECK TO SEE IF STATE OF SENSOR IS OPEN
057A C625         CARMEE:  ADI  37
057C CD3A04                CALL TIERR
057F 79                    MOV  A,C
0580 E601                  ANI  1
0582 C2E300                JNZ  CARM       ;IF OPEN LEAVE ERROR CODE ON STACK
0585 CD0903                CALL RSTB       ;ELSE DELETE ERROR CODE FROM STACK
0588 C3E300                JMP  CARM
                  ;CSEN: SEARCHES FOR SENSOR IN SENSOR STACK, IF PRESENT AND A ALARM
                  ;OCCURS FOR THE FIRST TIME THEN THE CARRY FLAG IS RESET ON RETURN,
                  ;OTHERWISE THE CARRY FLAG = 1
                  ;IF SENSOR IS PRESENT THEN THE ZERO FLAG IS RESET TO 0,
                  ;OTHERWISE THE ZERO FLAG IS SET TO 1
                  ;CSEN TAKES THE SUB TYPE OF A MESSAGE AND UPDATES THE STATUS BYTE
                  ;H,L = ADDR OF SENSOR
                  ;BIT 0 = LAST REPORTED STATE OF SENSOR
                  ;        (0 = SECURE, 1 = ALARM)
                  ;BIT 1 = (1 = ALARM AS OCCURED SINCE THE LAST 5 MIN. UPDATE OR
                  ;        A SECURE AS NOT BEEN GIVEN SINCE THE LAST ALARM, ELSE 0 = SECURE)
                  ;BIT 2 = PREVIOUS 5 MIN. UPDATE(SAME AS BIT 1 EXCEPT FOR
                  ;        THE PREVIOUS 5 MIN.)
                  ;BIT 4 = SENSOR MASK BIT (0 = SENSOR INCLUDED IN SYSTEM,
                  ;        1 = SENSOR MASKED FROM SYSTEM)
                  ;BIT 5 = SENSOR MESSAGE STATUS BIT FOR PRESENT HOUR
                  ;        1 = NO MESSAGES HAS OCCURED, 0 = A MESSAGE AS OCCURRED
                  ;BIT 6 = STATUS BIT FOR PREVIOUS HOUR
                  ;BIT 7 = STATUS ERROR BIT (0 = STATUS GOOD,1 = NO MESSAGES FOR PAST 2 HOURS)
                  ;SUB TYPE = BIT 0 IS THE PRESENT STATE OF THE SENSOR(SECURE=0,ALARM=1)
                  ;           BIT 1 IS 0 FOR HOURLY STATUS MESSAGE
                  ;                 IS 1 WHEN A CHANGE OF STATUS AS OCCURRED
                  ;NOTE(***)---A MESSAGE IS CHANGED FROM SECURE TO ALARM WHEN
                  ;        A SECURE MESSAGE FROM THE SENSOR IS NOT PRECEDED BY AN ALARM
                  ;        WITHIN THE PAST 10 MIN. AND LAST REPORTED STATE WAS SECURE)
058B 7E           CSEN:    MOV  A,M        ;LOAD SENSOR
058C 23                    INX  H
058D BA                    CMP  D          ;COMPARE INPUT WITH SENSOR
058E CA9805                JZ   CSEN1      ;IF MATCH, THEN UPDATE STATUS BYTE
0591 3C                    INR  A          ;ELSE CHECK FOR END OF SENSORS FLAG
0592 C28B05                JNZ  CSEN       ;IF NOT END OF SENSORS, THEN CHECK NEXT SENSOR
0595 AF                    XRA  A          ;IF END OF SENSOR, CLEAR CLEAR CARRY,AND SET ZERO
0596 4F                    MOV  C,A
0597 C9                    RET
0598 E5           CSEN1:   PUSH H          ;TEMPORARILY STORE SENSORS ADDR
0599 011D00                LXI  B,29
059C 09                    DAD  B          ;H,L = ADDR OF STATUS BYTE
059D 3A380C                LDA  SUBT       ;ACC = SUB TYPE
05A0 E603                  ANI  3
05A2 4F                    MOV  C,A        ;C = SUB TYPE
05A3 7E                    MOV  A,M        ;ACC = STAUS BYTE
05A4 47                    MOV  B,A
05A5 E616                  ANI  16H
05A7 B1                    ORA  C
05A8 77                    MOV  M,A        ;UPDATE STATUS BYTE
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ADDR OBJ-CODE LINENO.  SOURCE-STATEMENT

05A9 CD6909                  CALL IOPR1      ;CLEAR MESSAGE REGISTER
05AC E1                      POP  H
05AD E610                    ANI  10H        ;IF MASK BIT ON RETURN WITH NO ALARM
05AF C0                      RNZ
05B0 3A150C                  LDA  FTAMP      ;CHECK IF IN ACCESS MODE
05B3 3D                      DCR  A
05B4 C0                      RNZ             ;RETURN IF IN ACCESS MODE
05B5 78                      MOV  A,B
05B6 0F                      RRC
05B7 E602                    ANI  2
05B9 B0                      ORA  B
05BA 47                      MOV  B,A
05BB 79                      MOV  A,C
05BC 2F                      CMA
05BD 0F                      RRC
05BE B0                      ORA  B
05BF E601                    ANI  1          ;RETURN IF NEW CHANGE BIT IS 0
05C1 C0                      RNZ             ;OR OLD STATE BIT IS 1
05C2 78                      MOV  A,B
05C3 2F                      CMA
05C4 A1                      ANA  C
05C5 37                      STC
05C6 C0                      RNZ             ;ALARM IF EITHER BIT GOES FROM 0 TO 1
05C7 B4                      ORA  H          ;ELSE CLEAR CARRY AND ZERO = 0
                                             ;CARRY 0 = NO ALARM OR ALARM IN PROGRESS,
                                             ;CARRY 1 = ALARM
                                             ;ZERO 1 = SENSOR NOT IN STACK
05C8 C9                      RET             ;ZERO 0 = SENSOR IN STACK
                       ;FIRE ALARM ROUTINE
                       ;ACC = SENSOR NO. AND ERROR CODE
05C9 CD3804            FIRE: CALL TIERRA     ;STACK ERROR CODE OF TI STACK
05CC 3A4F0C                  LDA  MODE       ;LOAD ALARM MODE
05CF E680                    ANI  80H
05D1 C29506                  JNZ  TESTLT     ;IF TEST MODE LIGHT TEST LIGHT
05D4 3E10                    MVI  A,10H
05D6 CDE906                  CALL UPAL       ;UPDATE ALARM STATUS
05D9 CD1A0A                  CALL MTRANA     ;CHECK FOR MODEM OUTPUT
05DC 78                      MOV  A,B        ;ACC = OLD ALP
05DD E610                    ANI  10H
05DF C2E300                  JNZ  CARM       ;IF FIRE ALARM IN PROGRESS, THEN RETURN TO LOOP
05E2 3E01                    MVI  A,1        ;SET FIRE ALARM FLAG
05E4 322B0C                  STA  FTFIRE
05E7 2A130C                  LHLD TIME
05EA 112C01                  LXI  D,300
05ED 19                      DAD  D
05EE 22650C                  SHLD TFIRE      ;START TIMER
05F1 AF                      XRA  A
05F2 32490C                  STA  FIRBEL     ;RESET BELL OFF
05F5 C3E300                  JMP  CARM
                       ;INTRUSION ALARM AFTER 20 SEC. WARNING ALERT
05F8 3E04              GARI: MVI  A,4
05FA 32270C                  STA  PAL        ;STORE INTRUSION ALARM UPDATE (PAL)
05FD 21190C                  LXI  H,CET
0600 7E                      MOV  A,M        ;LOAD TI CODE FOR INTRUSION
0601 3600                    MVI  M,0        ;RESET TI CODE
```

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ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

0603 C31E06        881          JMP   GAR        ;GO TO GENERAL ALARM ROUTINE
                   882 ;SPECIAL ALARM
0606 3E01          883 GARS:    MVI   A,1
0608 32270C        884          STA   PAL        ;STORE ALARM UPDATE
060B 7A            885          MOV   A,D
060C C31E06        886          JMP   GAR
                   887 ;TAMPER ALARM
060F 3E02          888 GART:    MVI   A,2
0611 32270C        889          STA   PAL        ;STORE TAMPER ALARM IN ALARM UPDATE
0614 7B            890          MOV   A,E        ;ACC = ERROR CODE
0615 C31E06        891          JMP   GAR        ;GO TO GENERAL ALARM ROUTINE
                   892 ;PANIC ALARM
0618 3E08          893 GARP:    MVI   A,8
061A 32270C        894          STA   PAL        ;PAL = ALARM IN PROGRESS UPDATE
061D 7B            895          MOV   A,E
                   896 ;GENERAL ALARM ROUTINE
061E CD3804        897 GAR:     CALL  TIERRA     ;STACK ERROR CODE
0621 3A4F0C        898          LDA   MODE       ;CHECK FOR TEST MODE
0624 07            899          RLC
0625 DA9506        900          JC    TESTLT     ;LIGHT TEST LIGHT IF TEST MODE
0628 3A270C        901          LDA   PAL        ;LOAD NEW ALARM
062B CDE906        902          CALL  UPAL       ;UPDATE ALARM AND ALARM IN PROGRESS
062E CD1A0A        903          CALL  MTRANA     ;TRANSMIT TO MODEM(IF IN REMOTE MODE)
0631 78            904          MOV   A,B        ;ACC = OLD ALP
0632 A7            905          ANA   A
0633 CA4406        906          JZ    GAR2       ;IF NO ALARM IN PROGRESS THEN OUTPUT ALARM
0636 E612          907          ANI   12H        ;ELSE IF FIRE OR TAMPER ALARM IN PREOG., RETURN
0638 C2E300        908          JNZ   CARM
063B 3A270C        909          LDA   PAL
063E A8            910          XRA   B          ;IF PAST ALARM WAS A SPECIAL
063F E603          911          ANI   3          ;AND IF PRESENT ALARM IN PROGRESS IS
0641 CAE300        912          JZ    CARM       ;NOT A TAMPER OR SPECIAL, RETURN
                   913 ;OUTPUT ALARMS
0644 3A270C        914 GAR2:    LDA   PAL
0647 F678          915          ORI   120
0649 0F            916          RRC
064A DAC606        917          JC    MSGBS      ;IF SPECIAL THEN START ALERT(5 MIN.)
064D E602          918          ANI   2          ;CHECK FOR INTRUSION
064F CACC06        919          JZ    ALBEL      ;IF NOT AN INTRUSION THEN ALARM BELL
0652 3A4F0C        920          LDA   MODE       ;IF INTRUSION AND IN REMOTE MODE
0655 FE0D          921          CPI   0DH        ;THEN DO NOT SOUND ALARM OR ALERT
0657 DAE300        922          JC    CARM       ;RETURN TO MAIN LOOP IF REMOTE
065A 87            923          ADD   A
065B F2CC06        924          JP    ALBEL      ;IF LOC ALARM OR LOC/REMOTE TURN ON BELL
065E 3E1B          925          MVI   A,1BH      ;ELSE
0660 CD1303        926          CALL  RSTAP      ;RESET ALARM IN PROGRESS(INTRUSION)
0663 3E01          927          MVI   A,1
0665 C3AA06        928          JMP   MSGE       ;OR ALERT ON FOR 5 SEC.
                   929 ;INTRUSION ALARM
0668 3E04          930 INTRD:   MVI   A,4
066A 32270C        931          STA   PAL        ;STORE ALARM PROGRESS UPDATE
066D 3A930C        932          LDA   SENSOR
0670 3C            933          INR   A
0671 7A            934          MOV   A,D        ;ERROR CODE IN ACC
0672 C21E06        935          JNZ   GAR        ;IF AT LEAST 1 EC, THEN GO TO GENERAL ALARM ROUTINE
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ADDR OBJ-CODE LINENO.  SOURCE-STATEMENT

0675 3A4F0C        936            LDA   MODE        ;LOAD ALARM MODE
0678 E6C0          937            ANI   0C0H
067A 7A            938            MOV   A,D         ;ERROR CODE
067B C21E06        939            JNZ   GAR         ;IF MODES 1 OR 2 GO TO GENERAL ALARM ROUTINE
067E 3A260C        940            LDA   ALP         ;IS ALARM ALREADY IN PROGRESS?
0681 E61E          941            ANI   1EH         ;CHECK ALL BUT SPECIAL
0683 7A            942            MOV   A,D
0684 C21E06        943            JNZ   GAR         ;IF ALARM IN PROGRESS, THEN GO TO GEN. ALARM
0687 21190C        944            LXI   H,CET       ;CHECK TO SEE IF WARNING IS ON ALREADY
068A 7E            945            MOV   A,M
068B A7            946            ANA   A
068C C26E05        947            JNZ   CARME       ;IF WARNING ON IGNOR ALARM
068F 72            948            MOV   M,D         ;TEMP. STORE ERROR CODE
0690 3E05          949            MVI   A,5
0692 C3AA06        950            JMP   MSGB        ;SOUND ALERT 25 SECS BEFORE ALARM
                   951 ;TURN ON TEST LIGHT FOR 20 SEC
0695 3E01          952 TESTLT: MVI   A,1
0697 322A0C        953            STA   FTDISP
069A 2A130C        954            LHLD  TIME
069D 111400        955            LXI   D,20
06A0 19            956            DAD   D
06A1 22630C        957            SHLD  TDISP
06A4 3E7F          958            MVI   A,7FH
06A6 D320          959            OUT   20H
06A8 3E04          960            MVI   A,4         ;AND SOUND LOCAL ALERT FOR 20 SEC
                   961 ;START LOCAL ALERT FOR SPECIFIED SECONDS = ACC
06AA 322F0C        962 MSGB:    STA   FALCNT
06AD 32300C        963 MSGB1:   STA   ALCNT       ;STORE ORIGINAL SEC COUNT TO BE USED LATER
06B0 06EF          964 MSGB2:   MVI   B,0EFH      ;START LOCAL ALERT MESSAGE B
06B2 2A130C        965            LHLD  TIME        ;START TIMER
06B5 110500        966            LXI   D,5         ;5 SEC TIMER
06B8 19            967            DAD   D
06B9 225D0C        968            SHLD  TALT
06BC 3E01          969            MVI   A,1
06BE 322D0C        970            STA   FTALT
06C1 3E18          971            MVI   A,18H
06C3 C3DE06        972            JMP   ALO
                   973 ;SPECIAL LOCAL ALERT
06C6 322E0C        974 MSGBS:   STA   SALCNT      ;STORE SPECIAL ALERT COUNT
06C9 C3B006        975            JMP   MSGB2       ;GO TO ALERT ROUTINE
                   976 ;START BELL ALERT
06CC 3E01          977 ALBEL:   MVI   A,1
06CE 322C0C        978            STA   FTBEL
06D1 2A130C        979            LHLD  TIME
06D4 112C01        980            LXI   D,300
06D7 19            981            DAD   D
06D8 225B0C        982            SHLD  TBEL        ;BELL ALARM 5 MIN. TIMER
06DB 06FB          983            MVI   B,0FBH
06DD AF            984            XRA   A
06DE 21320C        985 ALO:     LXI   H,OUTAL
06E1 B6            986            ORA   M
06E2 A0            987            ANA   B
06E3 77            988            MOV   M,A
06E4 D330          989            OUT   30H         ;TURN ON BELL
06E6 C3E300        990            JMP   CARM
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 ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

                  991 ;UPAL: UPDATES ALARM STATUS BITS FOR MODEM TRANSMIT AND
                  992 ;UPDATES ALARM IN PROGRESS
 06E9 21260C      993 UPAL:   LXI  H,ALP
 06EC 46          994         MOV  B,M
 06ED B0          995         ORA  B          ;UPDATE ALARM IN PROGRESS STATUS
 06EE 77          996         MOV  M,A
 06EF 2B          997         DCX  H
 06F0 B6          998         ORA  M          ;UPDATE ALARM STATUS
 06F1 77          999         MOV  M,A
 06F2 C9         1000         RET
                 1001 ;MASK: SETS MASK BIT IN STATUS BYTE IF LAST STATE IS OPEN OR
                 1002 ;       STATUS ERROR OCCURRED
                 1003 ; ALSO SETS TIBIT IF A SENSOR IS MASKED
                 1004 ; ON RETURN B = NO. OF SENSORS NOT MASKED
 06F3 111E00     1005 MASK:   LXI  D,30       ;H,L = ARRAY OF STATUS BYTE
 06F6 2A540C     1006         LHLD HRSEN      ;D,E = CORRESPONDING SENSORS
 06F9 EB         1007         XCHG
 06FA 19         1008         DAD  D
 06FB 3A580C     1009         LDA  SENBOT
 06FE 93         1010         SUB  E
 06FF 3C         1011         INR  A
 0700 4F         1012         MOV  C,A        ;C = ARRAY COUNT
 0701 0600       1013         MVI  B,0        ;B = NO. OF SENSORS NOT MASKED
 0703 1A         1014 MASK1:  LDAX D          ;LOAD SENSOR
 0704 04         1015         INR  B
 0705 3C         1016         INR  A          ;IS THIS A SENSOR OR SEPERATOR
 0706 CA2207     1017         JZ   MASK2      ;IF THIS IS A SEPERATOR THEN GO TO NEXT SENSOR
 0709 7E         1018         MOV  A,M        ;LOAD STATUS BYTE
 070A E6EF       1019         ANI  0EFH       ;RESET MASK BIT
 070C 77         1020         MOV  M,A
 070D E681       1021         ANI  81H
 070F CA2307     1022         JZ   MASK3      ;IF STATUS ERROR OR ALARM STATE, MASK
 0712 3A4F0C     1023         LDA  MODE
 0715 07         1024         RLC
 0716 DA2307     1025         JC   MASK3      ;IF TEST MODE DO NOT MASK OUT
 0719 3EFF       1026         MVI  A,0FFH     ;SET TIBIT
 071B 321A0C     1027         STA  TIBIT
 071E 3E10       1028         MVI  A,10H
 0720 B6         1029         ORA  M          ;SET MASK BIT
 0721 77         1030         MOV  M,A
 0722 05         1031 MASK2:  DCR  B
 0723 23         1032 MASK3:  INX  H
 0724 13         1033         INX  D
 0725 0D         1034         DCR  C
 0726 C20307     1035         JNZ  MASK1
 0729 78         1036         MOV  A,B        ;ACC = NO. OF GOOD SENSORS
 072A C9         1037         RET
                 1038 ;KEY: CHECK COMBINATION
                 1039 ;NOTE---D,E CONTAIN NEW KEY (KNEW)
                 1040 ;THE FOLLOWING IS THE REFERENCE ARR FOR EACH KEY
 072B 01         1041 KARR:   DB   1
 072C 04         1042         DB   4
 072D 07         1043         DB   7
 072E 0A         1044         DB   10
 072F 02         1045         DB   2
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 ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

 0730 05           1046          DB    5
 0731 08           1047          DB    8
 0732 00           1048          DB    0
 0733 03           1049          DB    3
 0734 06           1050          DB    6
 0735 09           1051          DB    9
 0736 0B           1052          DB    11
 0737 2A0E0C       1053 KEY:     LHLD  KOLD       ;LOAD H,L WITH LAST KEY(S) PRESSED
 073A EB           1054          XCHG             ;H,L <> D,E
 073B 220E0C       1055          SHLD  KOLD       ;STORE KNEW INTO KOLD
 073E 7C           1056          MOV   A,H        ;KEY PRESSED = (KOLD XOR KNEW) ANDED KNEW
 073F AA           1057          XRA   D          ;RESULT IS PUT IN H,L
 0740 A2           1058          ANA   D
 0741 67           1059          MOV   H,A
 0742 7D           1060          MOV   A,L
 0743 AB           1061          XRA   E
 0744 A3           1062          ANA   E
 0745 6F           1063          MOV   L,A
 0746 29           1064          DAD   H          ;SHIFT KEYS LEFT TO LEFT JUSTIFY
 0747 29           1065          DAD   H
 0748 29           1066          DAD   H
 0749 29           1067          DAD   H
                   1068 ;CHECK FOR WHICH KEY AND IF ONLY ONE HAS BEEN DEPRESSED
 074A 110C00       1069          LXI   D,12       ;E = KEY COUNT
 074D 1D           1070 C1:      DCR   E
 074E FAD800       1071          JM    CREC       ;IF NO NEW KEY THEN RETURN
 0751 29           1072          DAD   H          ;SHIFT TO CARRY KEY BIT
 0752 D24D07       1073          JNC   C1         ;IF NOT PRESSED CHECK NEXT KEY BIT
 0755 7D           1074          MOV   A,L        ;ELSE CHECK FOR ANY OTHER KEYS PRESSED
 0756 B4           1075          ORA   H
 0757 C2D800       1076          JNZ   CREC      ;NOT ONLY ONE ,EXIT COMBO CHECK
 075A 212B07       1077          LXI   H,KARR     ;LOAD TOP OF KEY ARRAY
 075D 19           1078          DAD   D          ;MOVE TO KEY INDEX
 075E 56           1079          MOV   D,M        ;LOAD D WITH KEY NO.
 075F 2A330C       1080          LHLD  CURKEY     ;LOAD CURRENT COMBO
                   1081 ;UPDATE CURRENT COMBO
 0762 29           1082          DAD   H          ;SHIFT OUT PREVIOUS 4TH DIGIT
 0763 29           1083          DAD   H
 0764 29           1084          DAD   H
 0765 29           1085          DAD   H
 0766 7A           1086          MOV   A,D        ;PUT IN NEW DIGIT
 0767 B5           1087          ORA   L
 0768 6F           1088          MOV   L,A        ;H,L = NEW COMBO CURRENT
 0769 22330C       1089          SHLD  CURKEY     ;STORE NEW CURRENT COMBO
 076C EB           1090          XCHG
 076D 2A400C       1091          LHLD  COMB       ;LOAD CORRECT COMBO
                   1092 ; COMPARE COMBO
 0770 7D           1093          MOV   A,L
 0771 93           1094          SUB   E
 0772 7C           1095          MOV   A,H
 0773 CA7A07       1096          JZ    C5         ;IF COMBO NOT CORRECT EXIT COMBO CHECK
 0776 00           1097          NOP
 0777 C3D800       1098          JMP   CREC
 077A 92           1099 C5:      SUB   D
 077B C2D800       1100          JNZ   CREC      ;IF COMBO NOT CORRECT EXIT
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 ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

                    1101 ;COMBINATION CORRECT
 077E 32170C        1102          STA  ARMS       ;DISARM SENSORS
 0781 21FFFF        1103          LXI  H,0FFFFH   ;CLEAR CURRENT COMBINATION REGISTER
 0784 22330C        1104          SHLD CURKEY
 0787 C37300        1105          JMP  SACC       ;GO TO ACCESS MODE
                    1106 ;CHECK SUB TYPE FOR EC MESSAGE
 078A EB            1107 INEC:    XCHG
 078B CD6909        1108          CALL IOPR1      ;CLEAR MESSAGE REGISTER
 078E EB            1109          XCHG
 078F 3A380C        1110          LDA  SUBT       ;LOAD SUB TYPE
 0792 E603          1111          ANI  3            ;CHECK FOR ARM REQUEST
 0794 CA3A08        1112          JZ   REQ          ;IF SUB TYPE = 0, THE ARM REQUEST
 0797 3D            1113          DCR  A            ;CHECK FOR CONFIRM 1
 0798 CA7908        1114          JZ   CON1         ;IF SUB TYPE = 1, THE CONFIRM 1
 079B 111E00        1115          LXI  D,30
 079E 19            1116          DAD  D          ;H,L = ADDR OF STATUS BYTE
 079F 3D            1117          DCR  A            ;CHECK FOR CONFIRM 2
 07A0 CABE08        1118          JZ   CON2         ;IF SUB TYPE = 2, THE CONFIRM 2
                    1119 ;ELSE SUB TYPE = 3, CHECK COMBINATION
 07A3 4E            1120          MOV  C,M        ;C = CODE WORD
 07A4 3A390C        1121          LDA  IDDATA     ;LOAD ID DATA
 07A7 E60F          1122          ANI  0FH        ;MASK IN ENCODED NO.
 07A9 2A350C        1123          LHLD COMBEC       ;LOAD CURRENT EC COMBO
 07AC 29            1124          DAD  H            ;SHIFT IN NEW DIGIT(ID DATA)
 07AD 29            1125          DAD  H
 07AE 29            1126          DAD  H
 07AF 29            1127          DAD  H
 07B0 B5            1128          ORA  L
 07B1 6F            1129          MOV  L,A
 07B2 22350C        1130          SHLD COMBEC       ;STORE NEW CURRENT COMBO
 07B5 EB            1131          XCHG
 07B6 21100C        1132          LXI  H,KEYCNT   ;CHECK KEY COUNT
 07B9 34            1133          INR  M
 07BA 7E            1134          MOV  A,M
 07BB FE04          1135          CPI  4          ;IF KEY COUNT IS NOT >= 4 THEN
 07BD DAE300        1136          JC   CARM       ;RETURN TO MAIN LOOP
 07C0 2A400C        1137          LHLD COMB       ;LOAD CORRECT COMBINATION
                    1138 ; COMPARE COMBO WITH ENCODED CORRECT COMBO
 07C3 CD0F08        1139          CALL DECOD      ;DECODE COMB. AND CHECK IF IT IS CORRECT
 07C6 CAD507        1140          JZ   COK        ;COMBINATION CORRECT GO TO COK
                    1141 ;COMPARE COMBO WITH ENCODED WORD REVERSED
 07C9 79            1142          MOV  A,C
 07CA 07            1143          RLC
 07CB 07            1144          RLC
 07CC 07            1145          RLC
 07CD 07            1146          RLC
 07CE 4F            1147          MOV  C,A
 07CF CD0F08        1148          CALL DECOD
 07D2 C2E300        1149          JNZ  CARM           ;LOWER HALF OF COMBO CORRECT GO INTO ACCESS
                    1150 ;COMBINATION OK TRANSMIT STRIKE RELEASE
 07D5 211A0C        1151 COK:     LXI  H,TIBIT
 07D8 7E            1152          MOV  A,M
 07D9 E60F          1153          ANI  0FH
 07DB 5F            1154          MOV  E,A        ;E = TIBIT
 07DC AF            1155          XRA  A
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ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

07DD 32100C               STA  KEYCNT       ;RESET KEY COUNT
07E0 322F0C               STA  FALCNT       ;RESET ALERT
07E3 32170C               STA  ARMS         ;DISARM SENSORS
               ;
               ;NOTE---FOLLOWING STATEMENT SHOULD BE A NOP TO INSURE AGAINST THE LOSS
               ;          OF STRIKE RELEASE AND TI INDICATOR
               ;          CHANGE 'MOV  M,A' TO 'NOP'
               ;
07E6 77                   MOV  M,A          ;RESET TIBIT
               ;
07E7 57                   MOV  D,A          ;D = SUB TYPE = STRIKE RELEASE
07E8 3A370C               LDA  TYPE
07EB E607                 ANI  7
07ED F608                 ORI  8            ;ACC = TYPE = EC NO.
07EF CD710A               CALL TRANS        ;TRANSMIT STRIKE RELEASE BACK TO EC
               ;CHECK ALARM IN PROGRESS
07F2 0604                 MVI  B,4
07F4 21490C               LXI  H,FIRBEL     ;SET FIRE BELL OFF
07F7 70                   MOV  M,B
07F8 3A180C               LDA  FTSW         ;IF TAMPER ALARM THEN DO NOT TURN OFF BELL
07FB 3D                   DCR  A
07FC A0                   ANA  B
07FD 47                   MOV  B,A
07FE 21320C               LXI  H,OUTAL
0801 7E                   MOV  A,M
0802 B0                   ORA  B
0803 77                   MOV  M,A
0804 D330                 OUT  30H
0806 05                   DCR  B
0807 3E01                 MVI  A,1
0809 F41303               CP   RSTAP        ;IF NO TAMPER, THEN RESET ALP
080C C3E300               JMP  CARM         ;RETURN TO MAIN LOOP CHECK ARM BUTTON
               ;DECODE D,E USING REG. C AS CODE WORD AND COMPARE WITH H,L
               ;ZERO = 1 IF COMBINATION IS CORRECT
080F 79        DECOD:     MOV  A,C          ;XOR FIRST HALF
0810 AB                   XRA  E
0811 95                   SUB  L            ;CHECK COMB.
0812 C0                   RNZ               ;RETURN IF NOT EQUAL
0813 79                   MOV  A,C
0814 AA                   XRA  D            ;CHECK SECOND HALF
0815 94                   SUB  H
0816 C9                   RET
               ;UPDATE PERIMETER SENSOR STATE
0817 3A370C    UP:        LDA  TYPE         ;LOAD TYPE
081A E603                 ANI  3
081C C64C                 ADI  4CH          ;GET PERIMETER SENSOR NO.
081E 4F                   MOV  C,A
081F 21930C               LXI  H,SENSOR     ;TOP OF SENSOR STACK
0822 111E00               LXI  D,30
0825 23        UP1:       INX  H
0826 BE                   CMP  M
0827 C22508               JNZ  UP1          ;LOOP THAT FINDS SENSOR IN STACK
082A 19                   DAD  D            ;D = ADDR OF STATUS BYTE
082B 7E                   MOV  A,M          ;SET STATUS BYTE USING B REG
082C E6FC                 ANI  0FCH
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ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

082E B0                        ORA   B
082F 77                        MOV   M,A
0830 79                        MOV   A,C
0831 C625                      ADI   37
0833 CD3A04           UP2:     CALL  TIERR      ;DELETE DOOR OPEN ERROR CODE
0836 CD0903                    CALL  RSTB       ;RESET TI BIT IF NO ERROR CODES
0839 C9                        RET
                      ;ARM REQUEST
083A 3A4F0C           REQ:     LDA   MODE       ;LOAD MODE
083D 5F                        MOV   E,A
083E 3A150C                    LDA   FTAMP      ;IF IN ACCESS MODE THEN DO NOT ARM
0841 3D                        DCR   A
0842 B3                        ORA   E
0843 E684                      ANI   84H        ;IF FIRE/PANIC OR TEST MODES SET TROUBLE
0845 3E59                      MVI   A,89       ;ERROR CODE FOR TROUBLE
0847 CA5008                    JZ    REQ1
084A CD3A04                    CALL  TIERR      ;CALL TROUBLE INDICATOR ROUTINE
084D C3E300                    JMP   CARM       ;RETURN TO MAIN POLLING LOOP
0850 224A0C           REQ1:    SHLD  ECSS       ;STORE TOP OF STACK
0853 0664                      MVI   B,100      ;DELETE ERROR CODES BETWEEN 0 AND 100
0855 CDEC02                    CALL  RTI
0858 3A4F0C                    LDA   MODE       ;ACC = MODE
085B E640                      ANI   40H        ;IF ALARM MODE 2, THEN SET TROUBLE BIT
085D 3E58                      MVI   A,88       ;ERROR CODE FOR TROUBLE
085F C43A04                    CNZ   TIERR      ;NO TROUBLE IF NOT LOCAL ALERT
0862 0602                      MVI   B,2        ;SET STATUS BYTE TO CLOSED
0864 CD1708                    CALL  UP
0867 CDF306                    CALL  MASK
086A 3E01                      MVI   A,1
086C 324E0C                    STA   X          ;X = 1
086F 2A4A0C                    LHLD  ECSS       ;H,L = CURRENT EC
0872 224C0C                    SHLD  ECSP       ;SET EC HANDSHAKE STACK POINTER
0875 7E                        MOV   A,M
0876 C34103                    JMP   SAR2
                      ;CONFIRM 1
0879 3A160C           CON1:    LDA   VARM       ;LOAD VARM
087C 3D                        DCR   A          ;IS VARM = 1
087D C2E300                    JNZ   CARM       ;IF VARM IS NOT = 1, GO BACK TO MAIN LOOP
0880 3A390C                    LDA   IDDATA     ;LOAD CODE WORD FROM EC
0883 E60F                      ANI   0FH        ;MASK IN
0885 5F                        MOV   E,A
0886 3A420C                    LDA   CODE         ;LOAD CODE WORD
0889 57                        MOV   D,A
088A E60F                      ANI   0FH          ;MASK IN 1ST HALF OF CODE WORD
088C BB                        CMP   E            ;DO CODE AND DATA MATCH?
088D C2E803                    JNZ   ECERR      ;IF CODE NO. DOES NOT AGREE, GO TO REPEAT MESSAGE
0890 3E01                      MVI   A,1
0892 32290C                    STA   FTCODE     ;START CODE TIMER
0895 7A                        MOV   A,D          ;AND TRANSMIT 2ND HALF OF CODE WORD
0896 2A130C                    LHLD  TIME
0899 23                        INX   H
089A 23                        INX   H
089B 22610C                    SHLD  TCODE
089E 07                        RLC
089F 07                        RLC
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ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

08A0 07                      RLC
08A1 07                      RLC
08A2 E60F                    ANI   0FH
08A4 5F                      MOV   E,A
08A5 1602                    MVI   D,2
08A7 3A370C                  LDA   TYPE
08AA E60F                    ANI   0FH
08AC F608                    ORI   8
08AE CD710A                  CALL  TRANS
08B1 3E02                    MVI   A,2
08B3 32160C                  STA   VARM
08B6 3E04                    MVI   A,4
08B8 32310C                  STA   REP
08BB C3E300                  JMP   CARM        ;GO TO MAIN LOOP, VARM=2, REP=4
                  ;CONFIRM 2
08BE 3A160C       CON2:      LDA   VARM        ;CHECK FOR VARM = 2
08C1 FE02                    CPI   2
08C3 C2E300                  JNZ   CARM        ;IF VARM NOT = 2 , RETURN TO MAIN LOOP
08C6 3A390C                  LDA   IDDATA      ;LOAD CODE WORD FROM EC
08C9 E60F                    ANI   0FH
08CB 5F                      MOV   E,A
08CC 3A420C                  LDA   CODE          ;LOAD CODE WORD
08CF 57                      MOV   D,A
08D0 07                      RLC
08D1 07                      RLC
08D2 07                      RLC
08D3 07                      RLC
08D4 E60F                    ANI   0FH           ;MASK IN 2ND HALF OF CODE WORD
08D6 BB                      CMP   E             ;DO CODE AND DATA MATCH?
08D7 C2E803                  JNZ   ECERR       ;IF NO MATCH THEN EC ERROR
08DA 72                      MOV   M,D         ;STORE NEW CODE WORD
08DB AF                      XRA   A
08DC 32160C                  STA   VARM        ;RESET VARM
08DF 32290C                  STA   FTCODE      ;TURN OFF CODE TIMER
08E2 1603                    MVI   D,3
08E4 3A1A0C                  LDA   TIBIT
08E7 E60F                    ANI   0FH
08E9 5F                      MOV   E,A
08EA 3A370C                  LDA   TYPE
08ED E60F                    ANI   0FH
08EF F608                    ORI   8
08F1 CD710A                  CALL  TRANS       ;TRANSMIT TO EC, TROUBLE BIT AND OK
08F4 CD750A                  CALL  TRAN2       ;TRANSMIT A 2ND OK MESSAGE
08F7 C32C03                  JMP   SARM
                  ;IOPOLL: CHECK FOR RECEIVER DATA FROM POWER LINE OR MODEM
                  ;        AND TRANSMIT DATA ON MODEM
                  ;        ROUTINE LOOKS FOR RISING EDGE OF CLOCK, IF NOT
                  ;        RISING EDGE THEN IT IMMEDIATLY RETURNS, ELSE CHECK FOR
                  ;        ANY I/O TO BE DONE
08FA 213A0C       IOPOLL:    LXI   H,INTF      ;LOAD LAST STATE OF CLOCK
08FD 5E                      MOV   E,M
08FE DB30                    IN    30H         ;INPUT CLOCK
0900 57                      MOV   D,A
0901 77                      MOV   M,A         ;STORE NEW CLOCK STATE
0902 2F                      CMA
```

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ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

0903 E640       1321          ANI  40H        ;MASK IN CLOCK BIT
0905 A3         1322          ANA  E          ;CHECK FOR RISING EDGE
0906 C8         1323          RZ              ;IF NOT RISING EDGE, THEN RETURN
                1324 ;UPDATE SECOND TIMER
0907 21120C     1325          LXI  H,TCNT     ;LOAD TIME COUNT
090A 7E         1326          MOV  A,M
090B 3C         1327          INR  A
090C 77         1328          MOV  M,A        ;INCREMENT COUNT
090D E63F       1329          ANI  3FH
090F C21909     1330          JNZ  IOT        ;EVERY 32 INCREMENTS ADD 1 TO SEC TIMER
0912 2A130C     1331          LHLD TIME       ;SEC TIMER
0915 23         1332          INX  H
0916 22130C     1333          SHLD TIME       ;SEC TIMER + 1
                1334 ;CHECK FOR MODEM DATA
0919 3A150C     1335 IOT:     LDA  FTRMP      ;IF EITHER IN ACCESS MODE
091C 214F0C     1336          LXI  H,MODE     ;OR NON-REMOTE MODE, THEN IGNOR MODEM
091F 3D         1337          DCR  A
0920 2F         1338          CMA
0921 A6         1339          ANA  M
0922 21240C     1340          LXI  H,MTEND    ;ADDR OF END-MODEM-TRANS FLAG
0925 E618       1341          ANI  18H
0927 CA3A09     1342          JZ   IOIGN      ;RESET FMTR IF IGNOR MODEM
092A 7A         1343          MOV  A,D
092B E620       1344          ANI  20H        ;MASK IN CARRIER
092D CA3D09     1345          JZ   IOMT       ;IF NO CARRIER, THEN TRANSMIT MODEM DATA
                1346 ;CHECK TO SEE IF INTERIGATION AS BEEN COMPLETED ALREADY
0930 7E         1347          MOV  A,M        ;LOAD END-MODEM-TRANS FLAG
0931 A7         1348          ANA  A
0932 0680       1349          MVI  B,80H      ;B = HARDWARE FLAG OUTPUT
0934 CA7809     1350          JZ   IOMR       ;IF INTERIGATION NOT FINISHED, GET REC DATA
0937 C34609     1351          JMP  IOPR       ;ELSE CHECK FOR POWER LINE DATA
093A 32220C     1352 IOIGN:   STA  FMTR       ;RESET TRANSMITTER FLAG
093D AF         1353 IOMT:    XRA  A
093E 77         1354          MOV  M,A        ;RESET FLAG FOR NEXT INTERIGATION
                1355 ;CHECK FOR DATA TO BE TRANSMITTED TO MODEM
093F 3A220C     1356          LDA  FMTR
0942 A7         1357          ANA  A
0943 C22D0A     1358          JNZ  MTRAN      ;TRANSMIT TO MODEM, IF NO CARRIER
                1359 ;CHECK FOR JAMMING
0946 7A         1360 IOPR:    MOV  A,D
0947 07         1361          RLC             ;CHECK PHASE LOCK
0948 DA7609     1362          JC   REC        ;IF PHASE LOCK GO GET POWER LINE DATA
094B 21320C     1363          LXI  H,OUTAL    ;SWITCH TO 60 HZ TRANSMITTER CLOCK
094E 3E81       1364          MVI  A,81H
0950 B6         1365          ORA  M
0951 E6FD       1366          ANI  0FDH
0953 77         1367          MOV  M,A
0954 D330       1368          OUT  30H
0956 2A130C     1369          LHLD TIME       ;ELSE SET TIMER TO RECORD LAST TIME NO PHASE
0959 01AE00     1370          LXI  B,174      ;LOCK OCCURRED
095C 09         1371          DAD  B          ;STORE JAMMING 3 MIN. TIMER
095D 22430C     1372          SHLD TJAM
0960 21110C     1373          LXI  H,FJAM     ;RESET TI JAMMING ERROR CODE
0963 34         1374          INR  M
0964 70         1375          MOV  M,B        ;RESET JAMMING FLAG TO ZERO
```

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ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

0965 79                   MOV  A,C
0966 FC3308               CM   UP2          ;RESET JAMMING CODE IF JAMMING ALARM
0969 21FFFF      IOPR1:   LXI  H,0FFFFH     ;CLEAR RECEIVER REGISTER
096C 221C0C               SHLD RMESS
096F 221E0C               SHLD RMESS2
0972 22200C               SHLD RMESS4
0975 C9                   RET
                 ;RECEIVE DATA FROM POWER LINE (B = 1) OR MODEM (B = 80 HEX)
                 ;AND CHECK ID AND PARITY
0976 0601        REC:     MVI  B,1
0978 21320C      IOMR:    LXI  H,OUTAL
097B 7E                   MOV  A,M
097C E67C                 ANI  07CH
097E B0                   ORA  B
097F 77                   MOV  M,A          ;SET POWER LINE RECEIVER FLAGS
0980 D330                 OUT  30H          ;OUTPUT FLAGS TO HARDWARE
0982 211C0C               LXI  H,RMESS
0985 DB10                 IN   10H          ;INPUT DATA
0987 0F                   RRC
0988 7E                   MOV  A,M          ;STORE PARITY BIT
0989 17                   RAL
098A 77                   MOV  M,A
                 ;ROTATE TO GET ID FIELD
098B 1F                   RAR
098C 1F                   RAR
098D 23                   INX  H            ;LOAD OLD ID FIELD
098E 7E                   MOV  A,M
098F 17                   RAL               ;SHIFT IN NEW BIT
0990 77                   MOV  M,A          ;STORE NEW ID
0991 57                   MOV  D,A          ;TEMPORARILY STORE 2ND HALF OF ID
0992 23                   INX  H
0993 05                   DCR  B
0994 CAA109               JZ   RECP         ;IF B = 1, THEN SHIFT BIT INTO TYPE,SUB,IDDATA
0997 3EFF                 MVI  A,0FFH       ;SET TYPE,SUB TYPE AND ID DATA TO ALL 1'S
0999 77                   MOV  M,A
099A 23                   INX  H
099B 77                   MOV  M,A
099C 23                   INX  H
099D 77                   MOV  M,A
099E C3B709               JMP  RECM         ;ELSE DO NOT SHIFT INTO TYPE,SUB TYPE,IDDATA
09A1 7E          RECP:    MOV  A,M          ;LOAD OLD ID DATA
09A2 17                   RAL
09A3 77                   MOV  M,A          ;STORE NEW ID DATA
09A4 23                   INX  H
09A5 17                   RAL
09A6 17                   RAL
09A7 17                   RAL
09A8 17                   RAL
09A9 7E                   MOV  A,M          ;LOAD OLD SUB TYPE
09AA 17                   RAL
09AB 77                   MOV  M,A          ;STORE NEW SUB TYPE
09AC 23                   INX  H
09AD 1F                   RAR
09AE 1F                   RAR
09AF 1F                   RAR
```

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PAGE = 27          7/ 3/76          15:21:19
 ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

 09B0 7E                       MOV   A,M         ;LOAD OLD TYPE
 09B1 17                       RAL
 09B2 77                       MOV   M,A         ;STORE NEW TYPE
 09B3 17                       RAL
 09B4 17                       RAL
 09B5 17                       RAL
 09B6 17                       RAL
 09B7 23                 RECM: INX   H
 09B8 7E                       MOV   A,M
 09B9 17                       RAL
 09BA 77                       MOV   M,A         ;STORE NEW ID
 09BB D8                       RC                ;IF A 0 DOES NOT PRECEDE MESSAGE, THEN RETURN
 09BC 2A3E0C                   LHLD  ID          ;COMPARE ID FIELDS WITH CORRECT ID
 09BF 94                       SUB   H
 09C0 5F                       MOV   E,A
 09C1 7A                       MOV   A,D
 09C2 95                       SUB   L
 09C3 B3                       ORA   E
 09C4 C0                       RNZ               ;RETURN IF NO ID MATCH
                         ;CHECK PARITY
 09C5 1600                     MVI   D,0
 09C7 211C0C                   LXI   H,RMESS
 09CA 7E                       MOV   A,M
 09CB 5F                       MOV   E,A
 09CC 23                       INX   H
 09CD 7E                       MOV   A,M
 09CE A7                       ANA   A           ;CHECK RMESS1 PARITY
 09CF EAD309                   JPE   REPL1
 09D2 14                       INR   D
 09D3 23                 REPL1: INX  H
 09D4 7E                       MOV   A,M         ;CHECK RMESS2 PARITY
 09D5 E60F                     ANI   0FH
 09D7 EADB09                   JPE   REPL2
 09DA 14                       INR   D
 09DB 23                 REPL2: INX  H
 09DC 7E                       MOV   A,M
 09DD E63F                     ANI   3FH         ;CHECK RMESS3,4 PARITY
 09DF EAE309                   JPE   REPL3
 09E2 14                       INR   D
 09E3 23                 REPL3: INX  H
 09E4 23                       INX   H
 09E5 7E                       MOV   A,M
 09E6 A7                       ANA   A           ;CHECK RMESS5 PARITY
 09E7 EAEB09                   JPE   REPL4
 09EA 14                       INR   D
 09EB 7A                 REPL4: MOV  A,D         ;ACC = MESSAGE PARITY
 09EC AB                       XRA   E
 09ED 0F                       RRC
 09EE D20B0A                   JNC   RECERR
 09F1 04                       INR   B
 09F2 3E01                     MVI   A,1
 09F4 FA2D0A                   JM    MTRAN       ;MODEM MESSAGE RECEIVED OUTPUT MESSAGE
                         ;PARITY OK MESSAGE RECEIVED
 09F7 32230C                   STA   FREC        ;SET RECEIVER FLAG READY TO 1
 09FA 2B                       DCX   H
```

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ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

09FB 7E          1486           MOV  A,M
09FC 11370C      1487           LXI  D,TYPE      ;STORE TYPE FIELD
09FF 12          1488           STAX D
0A00 13          1489           INX  D
0A01 2B          1490           DCX  H
0A02 7E          1491           MOV  A,M
0A03 EE03        1492           XRI  3
0A05 12          1493           STAX D           ;STORE SUB TYPE FIELD
0A06 13          1494           INX  D
0A07 2B          1495           DCX  H
0A08 7E          1496           MOV  A,M
0A09 12          1497           STAX D           ;STORE ID DATA FIELD
0A0A C9          1498           RET
                 1499 ;POWER LINE RECEIVER MESSAGE ERROR ROUTINE
0A0B 211B0C      1500 RECERR:   LXI  H,ERRCNT    ;LOAD ERROR COUNT
0A0E 7E          1501           MOV  A,M
0A0F 3C          1502           INR  A
0A10 77          1503           MOV  M,A         ;INCREMENT ERROR COUNT AND RESTORE
0A11 FE06        1504           CPI  6           ;COMPARE WITH MAX ERROR COUNT
0A13 C0          1505           RNZ              ;IF ERROR COUNT HAS NOT REACHED MAX, RETURN
0A14 3E56        1506           MVI  A,86        ;ERROR CODE FOR RECEIVER ERROR
0A16 CD3A04      1507           CALL TIERR
0A19 C9          1508           RET
                 1509 ;MTRAN: OUTPUT TO MODEM THE STATE OF SYSTEM
                 1510 ;X = ALARM BIT FIELD = 5 BITS---FIRE,PANIC,INTRUSION,TAMPER,SPECIAL
                 1511 ;I = ID FIELD
                 1512 ;P = PARITY BIT
                 1513 ;TRANSMIT TO MODEM 18 LEADING ZEROS TO ALLOW 300 MIL SEC DELAY
                 1514 ;MESSAGE TRANSMITTED IS 0IIIIIIIIXXXXXIIIIIIIIP00
0A1A 3A4F0C      1515 MTRANA:   LDA  MODE        ;LOAD MODE
0A1D E618        1516           ANI  18H
0A1F C8          1517           RZ               ;RETURN IF NOT IN REMOTE MODE
0A20 DB30        1518           IN   30H         ;CHECK CARRIER
0A22 E620        1519           ANI  20H         ;MASK IN CARRIER BIT
0A24 3E03        1520           MVI  A,3
0A26 CA2D0A      1521           JZ   MTRAN       ;IF CARRIER IS ON, THEN RETURN
0A29 32220C      1522           STA  FMTR        ;ELSE SET MODEM TRANSMIT FLAG AND
0A2C C9          1523           RET              ;RETURN
0A2D 3D          1524 MTRAN:    DCR  A
0A2E 32220C      1525           STA  FMTR
0A31 3C          1526           INR  A
0A32 32240C      1527           STA  MTEND
0A35 21320C      1528           LXI  H,OUTAL     ;SET MODEM TRANSMIT FLAGS
0A38 7E          1529           MOV  A,M
0A39 F683        1530           ORI  83H
0A3B 77          1531           MOV  M,A
0A3C D330        1532           OUT  30H         ;OUTPUT FLAGS TO HARDWARE
0A3E 210000      1533           LXI  H,0         ;ELSE GENERATE 300 MIL SEC DELAY
0A41 0E0A        1534           MVI  C,10
0A43 CD5A0A      1535           CALL CLOCK1      ;TRANSMIT 18 BITS (APPROX. 300 MIL SEC)
0A46 3A3F0C      1536           LDA  IDH         ;LOAD HIGH ID BYTE
0A49 6F          1537           MOV  L,A
0A4A 0E05        1538           MVI  C,5
0A4C CD5A0A      1539           CALL CLOCK1
0A4F 3A250C      1540           LDA  ALARM       ;LOAD ALARM BITS
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 ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

 0A52 5F                          MOV  E,A          ;E = ALARM BITS
 0A53 1600                        MVI  D,0
 0A55 C39A0A                      JMP  TRNCOM
                   ;CLOCK: OUTPUTS UPPER 8 BITS OF H,L SERIALLY
                   ;       ON THE LEADING EDGE OF THE CLOCK
 0A58 0E08         CLOCK:  MVI  C,8          ;BIT COUNT
 0A5A DB30         CLOCK1: IN   30H          ;LOOK FOR FALLING EDGE 1ST
 0A5C E640                 ANI  40H
 0A5E CA5A0A               JZ   CLOCK1
 0A61 DB30         CLOCK2: IN   30H          ;LOOK FOR RISING EDGE
 0A63 E640                 ANI  40H
 0A65 C2610A               JNZ  CLOCK2
 0A68 7C                   MOV  A,H          ;FALLING EDGE, MOVE H TO ACC
 0A69 D310                 OUT  10H          ;OUTPUT ACC TO TRANSMITTER
 0A6B 29                   DAD  H            ;SHIFT DATA LEFT
 0A6C 0D                   DCR  C            ;END OF BIT COUNT?
 0A6D C25A0A               JNZ  CLOCK1       ;GO TO NEXT BIT IF NOT END OF COUNT
 0A70 C9                   RET               ;ELSE RETURN
                   ;TRANS: TRANSMIT DATA OVER POWER LINES
                   ;ACC = TYPE
                   ;D = SUB TYPE
                   ;E = ID DATA
                   ;BIT FIELDS OF THE MESSAGE ARE AS FOLLOWS
                   ;T = TYPE FIELD BIT
                   ;I = ID FIELD BIT
                   ;S = SUB TYPE FIELD BIT
                   ;D = ID DATA FIELD BIT
                   ;P = PARITY BIT
                   ;NOTE---14 BITS ARE USED PRECEDING THE MESSAGE TO WAKE UP RECEIVER
                   ;          (10101010101010)
                   ;MESSAGE TRANSMITTED IS 10101010101010IIIIIIIITTTTSSDDDDIIIIIIIIP00
 0A71 07           TRANS:  RLC
 0A72 07                   RLC
 0A73 B2                   ORA  D
 0A74 57                   MOV  D,A          ;PUT TYPE AND SUB TYPE IN D REG
 0A75 21320C       TRAN2:  LXI  H,OUTAL      ;SET HARDWARE FLAGS FOR POWER LINE TRANSMITTER
 0A78 7E                   MOV  A,M
 0A79 E6FC                 ANI  0FCH
 0A7B F680                 ORI  80H
 0A7D 77                   MOV  M,A
 0A7E D330                 OUT  30H
 0A80 21AAAA               LXI  H,0AAAAH     ;H,L = 10101...
 0A83 0E06                 MVI  C,6
 0A85 CD5A0A               CALL CLOCK1       ;OUTPUT 14 LEADING BITS
 0A88 3A3F0C               LDA  IDH          ;LOAD HIGH ID BYTE
 0A8B 6F                   MOV  L,A
 0A8C 0E06                 MVI  C,6
 0A8E CD5A0A               CALL CLOCK1
 0A91 7A                   MOV  A,D
 0A92 B5                   ORA  L
 0A93 6F                   MOV  L,A          ;LOAD TYPE AND SUB TYPE
 0A94 0E04                 MVI  C,4
 0A96 CD5A0A               CALL CLOCK1
 0A99 7B                   MOV  A,E          ;LOAD ID DATA
 0A9A B5           TRNCOM: ORA  L
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ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

0A9B 6F                       MOV   L,A
0A9C CD580A                   CALL  CLOCK
0A9F 3A3E0C                   LDA   ID            ;LOAD LOW ID BYTE
0AA2 6F                       MOV   L,A
0AA3 0E03                     MVI   C,3
0AA5 CD5A0A                   CALL  CLOCK1
0AA8 3A3D0C                   LDA   IDPAR         ;GENERATE PARITY
0AAB 4F                       MOV   C,A
0AAC 7A                       MOV   A,D
0AAD A7                       ANA   A
0AAE EAB20A                   JPE   TR1
0AB1 0C                       INR   C
0AB2 7B                TR1:   MOV   A,E
0AB3 A7                       ANA   A
0AB4 EAB80A                   JPE   TR2
0AB7 0C                       INR   C
0AB8 79                TR2:   MOV   A,C
0AB9 2F                       CMA
0ABA 37                       STC
0ABB 17                       RAL                 ;SET A 1 AS LAST BIT OF MESSAGE
0ABC E603                     ANI   3
0ABE 37                       STC
0ABF 17                       RAL
0AC0 B5                       ORA   L
0AC1 6F                       MOV   L,A
0AC2 CD580A                   CALL  CLOCK
0AC5 CD580A                   CALL  CLOCK         ;TRANMIT REST OF MESSAGE
0AC8 21320C                   LXI   H,OUTAL       ;SET HARDWARE FLAGS TO REC POWER LINE
0ACB 7E                       MOV   A,M
0ACC E6FC                     ANI   0FCH
0ACE F681                     ORI   81H
0AD0 77                       MOV   M,A
0AD1 D330                     OUT   30H
0AD3 C36909                   JMP   IOPR1
                       ;
                       ;READ CODE PLUGS,COMBINATION,AND ID PLUG
                       ;STORE OLD STATUS AND RESET STATUS TO GOOD
0AD6 11930C            READCP: LXI  D,SENSOR      ;BEGINNING OF SENSORS IN THE SYSTEM
0AD9 21B10C                   LXI   H,STATUS      ;BEGINNING OF THE SENSOR STATUS
0ADC 01670C                   LXI   B,STOLD       ;BEGINNING OF OLDST ARRAY
                       ; STORE OLD CODE WORDS FOR EC
0ADF 3E1D                     MVI   A,29          ;MAX NO. OF SENSORS = 22
0AE1 323C0C            OLD1:  STA   COUNT         ;COUNT = NO. OF SENSORS
0AE4 1A                       LDAX  D             ;LOAD SENSOR NO. (TYPE AND ID DATA)
0AE5 13                       INX   D
0AE6 3C                       INR   A             ;IS BYTE A NULL BYTE
0AE7 CAF90A                   JZ    OLD3          ;IF NULL BYTE DO NOT STORE STATUS
0AEA 3D                       DCR   A
0AEB 02                       STAX  B             ;STORE AT OLDST
0AEC 03                       INX   B
0AED FE04                     CPI   4             ;CHECK FOR EC
0AEF 3EEF                     MVI   A,0EFH        ;RESET MASK BIT
0AF1 D2F60A                   JNC   OLD2          ;IF EC, THEN DO NOT RESET MASK BIT
0AF4 3EFF                     MVI   A,0FFH
0AF6 A6                OLD2:  ANA   M             ;INPUT STATUS (OR CODE WORD)
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ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

0AF7 02        1651         STAX B
0AF8 03        1652         INX  B
0AF9 3620      1653 OLD3:   MVI  M,20H      ;LOAD STATUS BYTE WITH GOOD
0AFB 23        1654         INX  H
0AFC 3A3C0C    1655         LDA  COUNT
0AFF 3D        1656         DCR  A          ;DECREMENT COUNT
0B00 C2E10A    1657         JNZ  OLD1       ;IF NOT END OF ARRAY, THEN GO TO OLD1
0B03 21930C    1658         LXI  H,SENSOR   ;H,L = TOP OF SENSOR LIST(STACK)
0B06 7D        1659         MOV  A,L
0B07 91        1660         SUB  C
0B08 3C        1661         INR  A
0B09 57        1662         MOV  D,A
0B0A 3EFF      1663         MVI  A,0FFH     ;FILL REST OF OLD STATUS WITH FF HEX
0B0C 02        1664 OLD4:   STAX B
0B0D 03        1665         INX  B
0B0E 15        1666         DCR  D
0B0F C20C0B    1667         JNZ  OLD4       ;LOOP THAT SETS REST OF ARRAY TO FF
               1668 ;READ CODE PLUGS OF THE EC'S
0B12 DB60      1669         IN   60H        ;EC,SPECIAL, AND PERIMETER PLUGS
0B14 224C0C    1670         SHLD ECSP       ;INITIALIZE STACK POINTER AT TOP OF STACK
0B17 224A0C    1671         SHLD ECSS
0B1A 0600      1672         MVI  B,0        ;B = 1ST EC
0B1C 50        1673         MOV  D,B
0B1D CDC60B    1674         CALL STOR2      ;STORE = CHECK CODE PLUG AND OLD STATUS
0B20 36FF      1675         MVI  M,0FFH
0B22 23        1676         INX  H
0B23 22560C    1677         SHLD STSEN      ;STORE BEGINNING OF SENSORS
0B26 06C0      1678         MVI  B,0C0H     ;STACK EC PANIC SENSORS
0B28 07        1679         RLC
0B29 07        1680         RLC
0B2A CDC60B    1681         CALL STOR2
0B2D 36FF      1682         MVI  M,0FFH     ;STORE SENSOR TYPE SEPERATOR
0B2F 23        1683         INX  H
0B30 06D0      1684         MVI  B,0D0H     ;STACK EC TAMPER SENSORS
0B32 07        1685         RLC
0B33 07        1686         RLC
0B34 CDC60B    1687         CALL STOR2
0B37 36FF      1688         MVI  M,0FFH
0B39 23        1689         INX  H
0B3A 22540C    1690         SHLD HRSEN      ;STORE BEGINNING OF HOUR STATUS SENSORS
0B3D 0670      1691         MVI  B,70H      ;STACK SPECIAL SENSORS
0B3F CDC60B    1692         CALL STOR2
0B42 36FF      1693         MVI  M,0FFH
0B44 23        1694         INX  H
0B45 0640      1695         MVI  B,40H      ;STACK PERIMETER SENSORS
0B47 CDC40B    1696         CALL STOR4
0B4A 064C      1697         MVI  B,4CH      ;STACK EC AS PERIMETER SENSORS
0B4C CDC60B    1698         CALL STOR2
0B4F 36FF      1699         MVI  M,0FFH
0B51 23        1700         INX  H
0B52 0650      1701         MVI  B,50H      ;STACK INTERNAL SENSORS
0B54 DBB0      1702         IN   0B0H
0B56 CDC40B    1703         CALL STOR4
0B59 36FF      1704         MVI  M,0FFH
0B5B 23        1705         INX  H
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 ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

 0B5C 0660                  MVI   B,60H       ;STACK FIRE SENSORS
 0B5E CDC40B                CALL  STOR4
 0B61 22580C                SHLD  SENBOT      ;STORE BOTTOM OF SENSOR STACK
 0B64 11B00C                LXI   D,STBOT     ;LOAD LIMIT OF STACK
 0B67 7B                    MOV   A,E
 0B68 95                    SUB   L
 0B69 3C                    INR   A
 0B6A 57                    MOV   D,A
 0B6B 3EFF                  MVI   A,0FFH
 0B6D 77              BOT:  MOV   M,A
 0B6E 23                    INX   H
 0B6F 15                    DCR   D
 0B70 C26D0B                JNZ   BOT         ;LOOP THAT SETS THE REST OF ARRAY TO FF
 0B73 CD990B                CALL  READM       ;READ MODE SWITCHES
                      ;READ ID PLUGS
 0B76 1600                  MVI   D,0
 0B78 DB40                  IN    40H
 0B7A 6F                    MOV   L,A
 0B7B A7                    ANA   A
 0B7C EA800B                JPE   RCP1
 0B7F 14                    INR   D           ;1ST HALF OF WORD IS ODD PARITY, D = 1
 0B80 DB50            RCP1: IN    50H
 0B82 67                    MOV   H,A
 0B83 A7                    ANA   A
 0B84 EA880B                JPE   RCP2
 0B87 14                    INR   D           ;IF 2ND HALF IS ODD D = D+1
 0B88 7A              RCP2: MOV   A,D
 0B89 323D0C                STA   IDPAR       ;STORE ID PARITY BIT
 0B8C 223E0C                SHLD  ID          ;STORE ID CODE
 0B8F DB90                  IN    90H         ;STORE CORRECT COMBINATION
 0B91 6F                    MOV   L,A
 0B92 DB80                  IN    80H
 0B94 67                    MOV   H,A
 0B95 22400C                SHLD  COMB        ;STORE 1ST AND 2ND HALF OF COMBO
 0B98 C9                    RET
                      ;READ MODE SWITCHES(SENSOR AND ALARM)
 0B99 DB70            READM: IN   70H
 0B9B 2F                    CMA
 0B9C 07                    RLC
                      ;READ ALARM MODE
 0B9D E6F0                  ANI   0F0H        ;MASK IN ALARM MODES
 0B9F 57                    MOV   D,A
 0BA0 67                    MOV   H,A
 0BA1 AF                    XRA   A           ;CLEAR ACC
 0BA2 5F                    MOV   E,A
 0BA3 29                    DAD   H
 0BA4 8B                    ADC   E
 0BA5 29                    DAD   H
 0BA6 8B                    ADC   E
 0BA7 29                    DAD   H
 0BA8 8B                    ADC   E
 0BA9 29                    DAD   H
 0BAA 8B                    ADC   E
 0BAB 3D                    DCR   A
 0BAC CAB20B                JZ    RM1         ;IF SUM OF MODES NOT = 1, MODE = TEST
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```
ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

0BAF 37                       STC
0BB0 1600                     MVI   D,0
0BB2 7A              RM1:     MOV   A,D
0BB3 1F                       RAR
0BB4 57                       MOV   D,A
                     ;READ SENSOR MODE
0BB5 DB70                     IN    70H
0BB7 2F                       CMA
0BB8 E603                     ANI   3
0BBA E2BF0B                   JPO   RM2          ;IF MODES ALL XOR DOORS/WINDOWS, RM2
0BBD 3E04                     MVI   A,4          ;ELSE MODE FIRE/PANIC
0BBF B2              RM2:     ORA   D
0BC0 324F0C                   STA   MODE         ;STORE MODES
0BC3 C9                       RET
                     ;STOREC: CHECKS FOR CODE PLUG MISSING
0BC4 14              STOR4:   INR   D            ;CHECK 4 SENSORS
0BC5 14                       INR   D
0BC6 14              STOR2:   INR   D            ;CHECK 2 SENSORS
0BC7 14                       INR   D
0BC8 0F              STORE:   RRC                ;CARRY EQUALS CODE PLUG PRESENTS
0BC9 D2D10B                   JNC   STO1         ;IF CODE PLUG PRESENT, DO NOT ADD TO SYSTEM
0BCC 70                       MOV   M,B          ;ELSE STORE SENSOR ON STACK
0BCD 23                       INX   H
0BCE CDD70B                   CALL  OLDST        ;CHECK FOR OLD STATUS
0BD1 04              STO1:    INR   B
0BD2 15                       DCR   D
0BD3 C2C80B                   JNZ   STORE        ;END OF LOOP
0BD6 C9                       RET
                     ;OLDST:  CHECK TO SEE IF THERE IS OLD STATUS PRESENT
                     ;IF SO,  THEN SET NEW STATUS = OLD STATUS
0BD7 D5              OLDST:   PUSH  D            ;TEMPORARILY STORE D,E
0BD8 4F                       MOV   C,A          ;TEMPORARILY STORE CODE PLUG INPUT
0BD9 78                       MOV   A,B          ;ACC = SENSOR
0BDA 0616                     MVI   B,22
0BDC 11670C                   LXI   D,STOLD      ;LOAD OLD STATUS ADDR
0BDF EB                       XCHG
0BE0 BE              OLST1:   CMP   M            ;LOOK FOR SENSOR
0BE1 CAEF0B                   JZ    OLST2        ;IF FOUND THEN SET NEW = OLD
0BE4 23                       INX   H
0BE5 23                       INX   H            ;ELSE GO TO NEXT SENSOR IN OLD STATUS
0BE6 05                       DCR   B
0BE7 C2E00B                   JNZ   OLST1        ;IF SENSOR NOT IN OLD STACK THEN NO CHANGE
0BEA 47                       MOV   B,A
0BEB 79                       MOV   A,C
0BEC EB                       XCHG
0BED D1                       POP   D            ;RESTORE D,E
0BEE C9                       RET
0BEF 23              OLST2:   INX   H            ;SET STATUS = OLD STATUS
0BF0 47                       MOV   B,A
0BF1 7E                       MOV   A,M
0BF2 211D00                   LXI   H,29
0BF5 19                       DAD   D
0BF6 77                       MOV   M,A
0BF7 79                       MOV   A,C
0BF8 EB                       XCHG
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ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

0BF9 D1                   POP  D
0BFA C9.                  RET
0BFB 00         ENDPRG: NOP
                ;LIST OF VARIABLES
0C00                      ORG  0C00H
                ;PROGRAM STACK
0C00            SK:       DS   14
                ; LAST KEY INPUT
0C0E 0000       KOLD:     DW   0
                ;KEY COUNT (COMBINATION OK IF COUNT > 3)
0C10 00         KEYCNT: DB   0
                ;FLAG FOR JAMMING (0 = NO ALARM YET, NOT 0 = ALARM ALREADY)
0C11 00         FJAM:     DB   0
                ;TIME COUNTER, INCREMENTED EVERY CLOCK PULSE
0C12 00         TCNT:     DB   0
                ;SECOND TIMER, WORD CONTAINING SECOND COUNT
                ;         INCREMENTED EVERY 64 TCNT INCREMENTS
0C13 0000       TIME:     DW   0
                ;TAMPER ENABLE: IF SET TAMPER IS ENABLED
0C15 00         FTAMP:    DB   0
                ;FLAG TELLING WHICH STATE OF HANDSHAKE(1 = CONFIRM 1, 2 = CONFIRM 2)
0C16 00         VARM:     DB   0
                ;SENSORS ARMED FLAG(0 = DISARMED,1 = ARMED)
0C17 00         ARMS:     DB   0
                ;FTSW: FLAG SET WHEN TAMPER
0C18 00         FTSW:     DB   0
                ;TEMPORARY STORAGE OF INTRUSION ERROR CODE DURING 25 SEC WARNING
0C19 00         CET:      DB   0
                ;TROUBLE BIT(0 = NO TROUBLE, FF = TROUBLE IN SYSTEM)
0C1A 00         TIBIT:    DB   0
                ;POWER LINE RECEIVER MESSAGE MESSAGE ERROR COUNT
0C1B 00         ERRCNT: DB   0
                ;BUFFER FOR POWER LINE RECEIVER SERIAL DATA
0C1C 00         RMESS:    DB   0            ;PARITY BIT
0C1D 00         RMESS1: DB   0              ;ID(LOWER)
0C1E 00         RMESS2: DB   0              ;ID DATA
0C1F 00         RMESS3: DB   0              ;SUB TYPE
0C20 00         RMESS4: DB   0              ;TYPE
0C21 00         RMESS5: DB   0              ;ID(UPPER)
                ;FLAG COUNT TO INDICATE THAT THE PROCESSOR IS WAITING TO TRANSMIT ON MODEM
0C22 00         FMTR:     DB   0
                ;RECEIVER DATA READY FLAG: SET IF RECEIVER MESSAGE IS PRESENT
0C23 00         FREC:     DB   0
                ;FLAG INDICATING THAT TRANSMISSION ON MODEM AS OCCURED
                ;AND ALL OTHER MESSAGES ON MODEM ARE TO BE IGNORED
                ;UNTIL CARRIER LIGHT HAS GONE OUT
0C24 00         MTEND:    DB   0
                ;ALARM BYTE(TRANSMITTED ON MODEM)
                ;BITS 0-4 = SPECIAL,TAMPER,INTRUSION,PANIC,FIRE
0C25 00         ALARM:    DB   0
                ;ALARM IN PROGRESS BYTE(SAME BITS AS ALARM:)
0C26 00         ALP:      DB   0
                ;ALARM IN PROGRESS UPDATE(USED BY GENERAL ALARM ROUT.,SAME AS ALARM:)
0C27 00         PAL:      DB   0
                ;TIMER FLAGS, 0 = TIMER NOT ON, ELSE NOT 0 = TIMER ON
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ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

0C28 00        1871 FTACC:  DB   0          ;ACCESS TIMER
0C29 00        1872 FTCODE: DB   0          ;EC 2 SEC HANDSHAKE TIMER
0C2A 00        1873 FTDISP: DB   0          ;PANEL DISPLAY TIMER
0C2B 00        1874 FTFIRE: DB   0          ;FIRE ALARM TIMER
0C2C 00        1875 FTBEL:  DB   0          ;LOCAL ALARM TIMER
0C2D 00        1876 FTALT:  DB   0          ;LOCAL ALERT TIMER
               1877 ;SPECIAL LOCAL ALERT COUNTER
0C2E 00        1878 SALCNT: DB   0
               1879 ;ORIGINAL LOCAL ALERT COUNTER
               1880 ; INDICATES WHAT TYPE OF ALERT (ARMING WARNING, SPECIAL, OR INTRUSION WARNING)
0C2F 00        1881 FALCNT: DB   0
               1882 ;GENERAL LOCAL ALERT COUNTER
0C30 00        1883 ALCNT:  DB   0
               1884 ;COUNTER FOR NO. OF TIMES A CONFIRM MESSAGE AS BEEN REPEATED
0C31 00        1885 REP:    DB   0
               1886 ;OUTPUT ALARM AND I/O BYTE: STORES STATE OF HARDWARE FLAGS
               1887 ;BIT 0 = 24, MODEM & POWER LINE INTERFACE
               1888 ;BIT 1 = 25,   "    "    "    "    "
               1889 ;BIT 2 = BELL ALARM
               1890 ;BIT 3 = FIRE ALARM BIT FOR ALERT
               1891 ;BIT 4 = TURN ON ALERT
               1892 ;BIT 5 = ACCESS LIGHT
               1893 ;BIT 6 = ARMED LIGHT
               1894 ;BIT 7 = 26, RECIEVER AND TRANSMIT CLOCK CONTROL(1=TRANS,0=REC)
0C32 00        1895 OUTAL:  DB   0
               1896 ;CURRENT INPUT COMBO
0C33 0000      1897 CURKEY: DW   0
               1898 ;CURRENT EC COMBINATION
0C35 0000      1899 COMBEC: DW   0
               1900 ;BITS OF THE TYPE, SUB TYPE, AND ID DATA FIELDS OF THE LAST RECIEVED MESSAGE
0C37 00        1901 TYPE:   DB   0          ;BITS 0-3 = TYPE FIELD
0C38 00        1902 SUBT:   DB   0          ;BITS 0,1 = SUB TYPE FIELD
0C39 00        1903 IDDATA: DB   0          ;BITS 0-3 = ID DATA FIELD
               1904 ;STORES THE LAST STATE OF CLOCK
0C3A 00        1905 INTF:   DB   0
               1906 ;STORES OLD ARM BUTTON POSITION
0C3B 00        1907 ABOLD:  DB   0
               1908 ;TEMPORARY STORAGE OF A COUNTER
0C3C 00        1909 COUNT:  DB   0
               1910 ;ID CODE PARITY BIT
0C3D 00        1911 IDPAR:  DB   0
               1912 ;ID CODE (READ FROM CODE PLUGS)
0C3E 00        1913 ID:     DB   0
0C3F 00        1914 IDH:    DB   0
               1915 ;CORRECT COMBO
0C40 00        1916 COMB:   DB   0          ;3RD AND 4TH DIGITS
0C41 00        1917 COMBH:  DB   0          ;1ST AND 2ND DIGITS
               1918 ;CODE WORD FOR ENCODING EC COMBINATION
0C42 00        1919 CODE:   DB   0
               1920 ;JAMMING TIMER
0C43 0000      1921 TJAM:   DW   0
               1922 ;5 MINUTE TIMER(FOR UPDATING SENSOR STATE)
0C45 0000      1923 MINS:   DW   0
               1924 ;HOUR TIMER(FOR UPDATING STATUS)
0C47 0000      1925 HOUR:   DW   0
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ADDR OBJ-CODE LINENO. SOURCE-STATEMENT

                    ;FIRE BELL FLAG (0 - FIRE BELL ON, 4 - OFF)
0C49 00.            FIRBEL: DB    0
                    ;BEGINNING POINTER FOR EC HANDSHAKE STACK(TOP OF QUEUE)
0C4A 0000           ECSS:    DW    0
                    ;PRESENT EC STACK POINTER
0C4C 0000           ECSP:    DW    0
                    ;FLAG FOR DETERMINING TO HANDSHAKE W/ OR W/O ARMING (0=NO ARMING,1=ARM)
0C4E 00             X:       DB    0
                    ;ALARM AND SENSOR MODE BYTE
                    ;BITS 0-2 = SENSOR MODE = ALL,EXTERNAL,FIRE/PANIC
                    ;BITS 3-7 = ALARM MODE = REMOTE,LOC/REMOTE,LOC ALARM,LOC ALERT,TEST
0C4F 00             MODE:    DB    0
                    ;TROUBLE INDICATOR STACK POINTER
                    ;  AFTER STACKING A TI CODE, TISP IS SET TO POINT AT THE TOP OF THE STACK
0C50 0000           TISP:    DW    0
                    ;POWER BIT:  SET FOR INIATIAL POWER UP
0C52 00             FPOW:    DB    0
                    ;RUN-SWITCH-ON BIT:  SET WHEN RUN SWITCH IS ALREADY ON WHEN POWERING UP
0C53 00             FRUN:    DB    0
                    ;POINTS TO BEGINNING OF SENSORS WITH STATUS MESSAGES
0C54 0000           HRSEN:   DW    0
                    ;POINTER FOR TOP OF SENSORS(NOT INCLUDING EC HANDSHAKE SENSORS)
0C56 0000           STSEN:   DW    0
                    ;BOTTOM OF SENSORS
0C58 0000           SENBOT:  DW    0
                    ;TISO: STORES ERROR CODE IN OUTPUT PORT 40H
0C5A 00             TISO:    DB    0
                    ;TIMERS, HOLDS TIME(SECONDS) WHEN TIMER EXPIRES
0C5B 0000           TBEL:    DW    0          ;LOCAL ALARM, 5 MIN.
0C5D 0000           TALT:    DW    0          ;LOCAL ALERT, 5 SEC * (SALCNT OR ALCNT)
0C5F 0000           TACC:    DW    0          ;ACCESS TIMER, 20 SEC
0C61 0000           TCODE:   DW    0          ;EC 2 SEC HANDSHAKE ERROR CHECK
0C63 0000           TDISP:   DW    0          ;DISPLAY, 20SEC
0C65 0000           TFIRE:   DW    0          ;FIRE ALARM, 5 MIN.
                    ;TEMPORARY STORAGE OF OLD STATUS BYTES
0C67                STOLD:   DS    44
                    ;TOP OF SENSOR LIST
                    ;        NOTE---GROUP OF SENSORS(E.C., PANIC, TAMPER, SPECIAL, PERIMETER,
                    ;                INTERNAL, AND FIRE) ARE SEPERATED BY A SEPERATOR BYTE = FF HEX
0C93                SENSOR:  DS    29
0CB0 00             STBOT:   DB    0          ;BOTTOM OF SENSORS
                    ;TOP OF LIST OF STATUS BYTES(CODE WORD FOR EC) OF SENSORS
0CB1                STATUS:  DS    29
                    ;BYTE BEFORE TI STACK
0CCE 00             TISTM:   DB    0
                    ;TOP OF TROUBLE INDICATOR STACK(ERROR CODES)
0CCF 00             TIST:    DB    0
0CD0                         END
```

SYMBOL TABLE

INT1	0015	INT2	0021	INT3	002C	WAIT	006A
SACC	0073	SACC1	00B6	CKEY	00C1	CREC	00D8
CARM	00E3	CTAMP	00F3	CTIM	011B	CTIM1	0126
CT1	0133	CT2	0145	CT3	0152	CT3A	0173
CT3B	0175	CT4	0184	CT5	01BB	CT6	01D1
CT7	01E3	CT8	01F9	CT9	0211	STM1	0235
CT10	0242	STU1	0267	STU3	028A	CT11	0293
ENDACC	02AD	CKTIM	02D3	CTIME	02DE	RTI	02EC
RTI1	02F2	RT2	02FA	RSTIB	02FF	RSTB	0309
RSTAL	0311	RSTAP	0313	RUNON	031B	SARK	0323
SARM	032C	SAR1	033B	SAR2	0341	SAR3	036E
SARL	0380	SAR4	0399	SAR5A	03A1	SAR5	03A4
SAR6	03AE	SARN	03C2	ECSU	03CA	ECSU1	03D3
ERREC	03D7	ERREC1	03E6	ECERR	03E8	ECERR1	0402
TISU	0426	TISU0	0431	TISU1	0434	TIERRA	0438
TIERR	043A	TIERR1	0443	TIERR2	044D	TIERR3	0457
TIERR4	0463	TIERR5	046E	ARMBUT	0474	AB1	0483
AB2	0495	AB3	0496	AB4	04A0	BCD	04C3
BCD1	04CF	RECDAT	04D8	RD0	04E2	RD1	0540
RDJAM	0546	RD2	055B	RD3	0568	CARME	056E
CARMEE	057A	CSEN	058B	CSEN1	0598	FIRE	05C9
GARI	05F8	GARS	0606	GART	060F	GARP	0618
GAR	061E	GAR2	0644	INTRD	0668	TESTLT	0695
MSGB	06AA	MSGB1	06AD	MSGB2	06B0	MSGBS	06C6
ALBEL	06CC	ALO	06DE	UPAL	06E9	MASK	06F3
MASK1	0703	MASK2	0722	MASK3	0723	KARR	072B
KEY	0737	C1	074D	C5	077A	INEC	078A
COK	07D5	DECOD	080F	UP	0817	UP1	0825
UP2	0833	REQ	083A	REQ1	0850	CON1	0879
CON2	08BE	IOPOLL	08FA	IOT	0919	IOIGN	093A
IOMT	093D	IOPR	0946	IOPR1	0969	REC	0976
IOMR	0978	RECP	09A1	RECM	09B7	REPL1	09D3
REPL2	09DB	REPL3	09E3	REPL4	09EB	RECERR	0A0B
MTRANA	0A1A	MTRAN	0A2D	CLOCK	0A58	CLOCK1	0A5A
CLOCK2	0A61	TRANS	0A71	TRAN2	0A75	TRNCOM	0A9A
TR1	0AB2	TR2	0AB8	READCP	0AD6	OLD1	0AE1
OLD2	0AF6	OLD3	0AF9	OLD4	0B0C	BOT	0B6D
RCP1	0B80	RCP2	0B88	READM	0B99	RM1	0BB2
RM2	0BBF	STOR4	0BC4	STOR2	0BC6	STORE	0BC8
STO1	0BD1	OLDST	0BD7	OLST1	0BE0	OLST2	0BEF
ENDPRG	0BFB	SK	0C00	KOLD	0C0E	KEYCNT	0C10
FJAM	0C11	TCNT	0C12	TIME	0C13	FTAMP	0C15
VARM	0C16	ARMS	0C17	FTSW	0C18	CET	0C19
TIBIT	0C1A	ERRCNT	0C1B	RMESS	0C1C	RMESS1	0C1D
RMESS2	0C1E	RMESS3	0C1F	RMESS4	0C20	RMESS5	0C21
FMTR	0C22	FREC	0C23	MTEND	0C24	ALARM	0C25
ALP	0C26	PAL	0C27	FTACC	0C28	FTCODE	0C29
FTDISP	0C2A	FTFIRE	0C2B	FTBEL	0C2C	FTALT	0C2D
SALCNT	0C2E	FALCNT	0C2F	ALCNT	0C30	REP	0C31
OUTAL	0C32	CURKEY	0C33	COMBEC	0C35	TYPE	0C37
SUBT	0C38	IDDATA	0C39	INTF	0C3A	ABOLD	0C3B
COUNT	0C3C	IDPAR	0C3D	ID	0C3E	IDH	0C3F
COMB	0C40	COMBH	0C41	CODE	0C42	TJAM	0C43
MINS	0C45	HOUR	0C47	FIRBEL	0C49	ECSS	0C4A
ECSP	0C4C	X	0C4E	MODE	0C4F	TISP	0C50
FPOW	0C52	FRUN	0C53	HRSEN	0C54	STSEN	0C56
SENBOT	0C58	TISO	0C5A	TBEL	0C5B	TALT	0C5D
TACC	0C5F	TCODE	0C61	TDISP	0C63	TFIRE	0C65
STOLD	0C67	SENSOR	0C93	STBOT	0C90	STATUS	0CB1
TISTM	0CCE	TIST	0CCF				

END